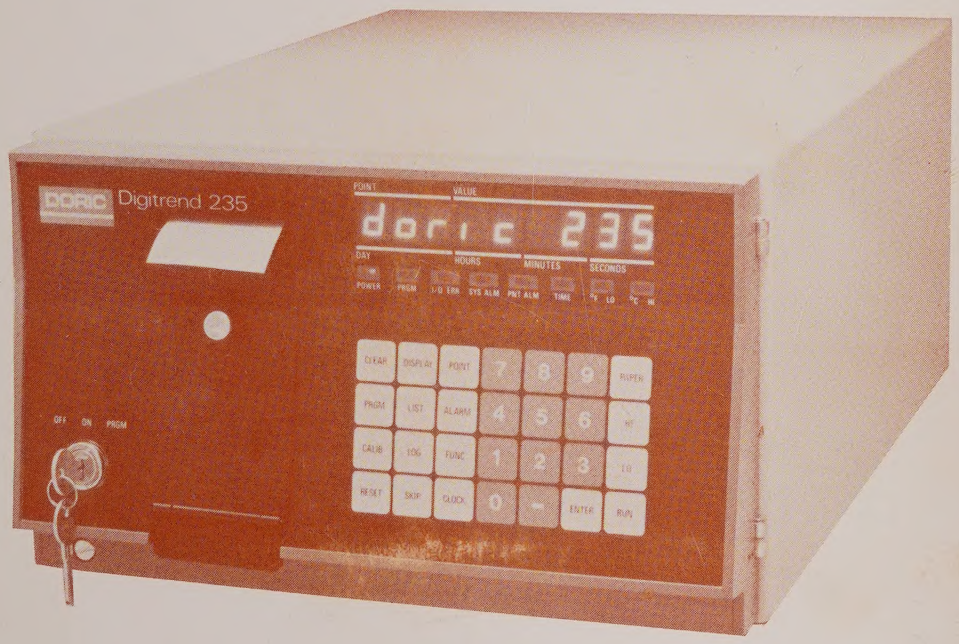
DORIC

M-466

STABRO LABORATORIES

MAINTENANCE MANUAL



Digitrend 235

WARRANTY

Doric Scientific hereby warrants each Digitrend® 235 as follows:

1. At the time of delivery of each instrument to the original purchaser, Doric Scientific UNCONDITIONALLY WARRANTS that it shall be free from defects in parts, materials and workmanship; and

2. Commencing with the date of shipments of each instrument to the original purchaser, Doric Scientific UNCONDITIONALLY WARRANTS that each unit shall remain free from defect in parts, materials and workmanship for a period of TWO YEARS.

In the event any instrument fails to meet the terms of this warranty, Doric Scientific agrees to provide corrective action. Refer to Warranty Claim (below) for proper procedure.

The warranties herein shall not obligate Doric Scientific in any manner whatsoever with respect to, and shall not be applicable to, any defects which after an inspection by Doric Scientific are not to Doric Scientific's reasonable satisfaction demonstrably the result of defective parts, materials or workmanship. We are not liable for consequential damages.

CERTIFICATION

Doric Scientific certifies that the instrument was thoroughly tested and inspected and found to meet its published specifications when shipped from the factory. Doric Scientific further certifies that its calibration measurements are traceable to NBS.

WARRANTY CLAIM

If either physical damage is found or operation is not within specification when the instrument is received, notify the carrier and Doric Scientific's Customer Service Department (619-565-4415) immediately. In the event the instrument fails to meet the terms of the warranty, Doric's Customer Service should be contacted for a plan of corrective action.

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EVENTS INPUTS (requires Option D and Option M)

CLEAR LOG # FUNC 103 HI RUN	*Enables high speed event interrupt and monitoring*
CLEAR LOG # FUNC 103 RUN	*Logs data from high speed event input buffer*
CLEAR RESET FUNC 103 HI RUN	*Aborts high speed event scan*
CLEAR RESET FUNC 103 RUN	*Aborts log of high speed buffer*

STATUS/EVENT INPUTS (requires Option D and Option M)

CLEAR LOG # FUNC 103 POINT #–# RUN	*Logs current state of status lines (one time demand log)*
CLEAR LOG # FUNC 103 POINT #–# CLOCK # RUN	*Logs current state of status lines on a periodic basis*
CLEAR RESET FUNC 103 LOG RUN	*Aborts logs of low speed status*

I/O CONTROL

CLEAR PRGM # PRGM RUN	*Enables program mode from I/O device 2 or 4*
CLEAR PRGM # RUN	*Disables programming capability from device 2 or 4*

PAPER FEED AND END OF FILE

CLEAR LOG # FUNC 101 RUN	*Gives paper feed/carriage return/file gap*
CLEAR RESET FUNC 101 RUN	*Aborts preceding process*

LINEAR SPECIAL SCALING $Y = MX + B$ **(requires Option M)**

CLEAR PRGM FUNC 107 ENT #M ENT #DEC ENT #O POINT #–# RUN	*For symbols and further details refer to Operator's Manual, pg 5-38*

POINT AVERAGE $AVG = \frac{PT_1 + PT_1 + PT_1 \cdots PT_1}{\text{time period}}$ **(requires Option M)**

Refer to Operators Manual, pg 5-33

CLEAR LOG # FUNC 106 POINT #–# CLOCK # RUN	*Sets averaging period*
CLEAR LOG # FUNC 106 POINT #–# RUN	*Reports last computed average*
CLEAR RESET FUNC 106 RUN	*Aborts averaging*

GROUP AVERAGE $AVG = \frac{PT_1 + PT_2 \ldots PT_n}{n}$ **(requires Option M)**

Refer to Operator's Manual, pg 5-40

CLEAR LOG # FUNC 109 POINT #–# RUN	*Logs average of points*
CLEAR LOG # FUNC 109 POINT #–# CLOCK # RUN	*Logs average of points on time interval*
CLEAR RESET FUNC 109 RUN	*Aborts group averaging*
CLEAR PRGM FUNC 109 ALARM # – # – # – # RUN*	*Assigns alarm limits to group average*
CLEAR PRGM FUNC 109 ALARM FUNC # – # – # – # RUN*	*Assigns alarm relays to group average*
CLEAR LIST # PRGM FUNC 109 RUN*	*Lists alarm assignments of group average*
CLEAR LOG # FUNC 109 POINT #–# ALARM RUN*	*Log average on alarm condition only*

POINT DIFFERENCE $DIFF = A - B$ **(requires Option M)**

CLEAR LOG # FUNC 104 POINT A# – A# ENT B# – B# RUN	*Log difference between A and B*
CLEAR LOG # FUNC 104 POINT A# – A# ENT B# – B# CLOCK # RUN	*Log difference periodically*
CLEAR LOG # FUNC 104 POINT A# – A# ENT B# – B# ALARM RUN*	*Log difference on alarm condition*
CLEAR PRGM FUNC 104 ALM # – # – # – # RUN*	*Assign limits to difference*
CLEAR PRGM FUNC 104 ALM FUNC # – # – # – # RUN*	*Assign relays to difference*
CLEAR LIST # PRGM FUNC 104 RUN*	*Printout alarm and relay assignments*

* requires Option A

GROUP AVERAGE ALARM LIMIT $L = \frac{PT_1 + PT_2 + PT_3 \ldots PT_n}{n} + K$ **(requires Option M and Option A)**

CLEAR PRGM FUNC 105 ENT #K POINT #–# HI/LO ALM #L RUN	*Sets up alarm limit #L as floating limit, high or low, equal to average of points #–# with added offset of K*
CLEAR RESET FUNC 105 RUN	*Abort floating alarm limit*

PERIPHERAL DEVICE ERROR DESCRIPTIONS

ERROR CODE	ERROR DESCRIPTION
Prnt Timeout	Printer halted for unknown reason; a restart was attempted after 10 sec.
Term1 Input	Serial I/O Port #1 input error: framing, overrun, or parity.
Term1 Output	Serial I/O Port #1 output error: Output buffer overflow or Clear to Send line pulled down for timeout period.
Term1 Line	Serial I/O Port #1 connection error: loss of carrier detected.
Term2 Input	Serial I/O Port #2 input error: framing, overrun, or parity.
Term2 Output	Serial I/O Port #2 output error: output buffer overflow or Clear to Send line pulled down for timeout period.
Term2 Line	Serial I/O Port #2 connection error: loss of carrier detected.
Tape Lost	Tape exist lost. Probable disconnected cable.
RTD FEM Cal	RTD FEM calibration error.
Tape Timeout	Tape READY timed out (there is a time limit in which the ready must come up).
Tape Write	Write error on magnetic tape.
Tape EOT	End of tape on magnetic tape. Tape low or broken on paper tape.
Unknown	I/O error of unknown cause.

FAULT MESSAGE DEFINITIONS

Fault message codes 001 through 025 are software generated diagnostic messages. Occasional occurences can be expected with no fatal problem in the system. If a message occurs repeatedly over a short period of time call Doric's Customer Service department for assistance.

COMMAND ERROR CODES

01	Command syntax error
02	Invalid Entry
03	Alarm option not present
04	Invalid command termination
05	Unable to execute command
06	Point Calib. gain too large
07	Not in calib. mode
08	Invalid device specification
09	No such function
10	Program key violation
11	Terminal input error
12	Status/event option not present
13	Point functions do not match
14	Point functions not calibratable
15	Too many differences entered
16	Points already being averaged

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DL26/3-82/500/SDP

DIGITREND® 235
COMMAND LIST

NOTES:

1. All commands must be preceded by CLEAR and terminated by RUN except HI LO and PAPER .
2. During command entry, the display echoes the keystrokes. After pressing RUN the display returns to its previous mode.
3. #–# may consist of:
   a. a single point or function number
   b. a first to last number
   c. up to 4 groups of first to last numbers are separated by ENTER or single numbers e.g.
   #–# ENTER #–# ENTER #–# ENTER #–#
   or
   # ENTER #–# ENTER #
4. The "#" after each log or list is an optional entry to select the output device. Output defaults to all devices in LOG mode and to requesting device only in LIST. The device code is as follows:
   1 = internal printer
   2 = serial I/O (std)
   3 = mag tape or paper tape (Opt. T or Opt. P)
   4 = serial I/O (Opt. S)
5. RESET may be used as a single keystroke edit or command entry.

DISPLAY JOGGING

HI	*Increments single point displayed or in calibration as long as pushed. Ignores skip*
LO	*Decrements single point displayed or in calibration as long as pushed. Ignores skip*

PAPER FEED AND LAMP TEST

PAPER	*Feeds paper and lights all LEDs/segments as long as pushed*

DEVICE DIAGNOSTIC

CLEAR LOG # FUNC 101 – #1 – #2 – #3 RUN	*Printer/output device test –#1 - Type of print: 1 = all same char: 2 = new character per row: 3 = diagonal alternating characters: #2 - numbers of lines printed (1-255), #3 - starting character 32-127, default is character 32 (blank)*
CLEAR RESET FUNC 101 RUN	*Aborts printer/output device test*

ALARM LIMITS (REQUIRES OPTION A)

CLEAR PRGM POINT #–# ALARM # – # – # – # RUN	*Assigns point group alarm limits (up to 4 per point)*
CLEAR PRGM ALARM #–# HI # RUN	*Programs alarm group as high limits of # (positive count)*
CLEAR PRGM ALARM #–# HI – # RUN	*Programs alarm group as high limit of negative #*
CLEAR PRGM ALARM #–# LO # RUN	*Programs alarm group as low limit of # (positive count)*
CLEAR PRGM ALARM #–# LO – # RUN	*Programs alarm group as low limit of negative #*
CLEAR PRGM ALARM #–# SKIP RUN	*Causes alarm to be skipped (temporarily made inactive although still assigned to points)*
CLEAR PRGM ALARM #–# SKIP – RUN	*Unskips alarm, causes alarm to return to active mode*
CLEAR DISPLAY PRGM ALARM #–# RUN	*Display alarm group values*
CLEAR LIST # PRGM ALARM #–# RUN	*List alarm group values*
CLEAR LIST # PRGM POINT #–# ALARM RUN	*List alarm/relay assignments for point group*
CLEAR LOG # POINT #–# ALARM RUN	*Log point group upon alarm transition within group*
CLEAR LOG # POINT #–# ALARM POINT RUN	*Log point in group when it makes alarm transition*
CLEAR LOG # POINT ALARM #–# RUN	*Log all points in alarm from group (one time demand log) or points returned or exceeded since last log*
CLEAR LOG # POINT ALARM #–# ALARM RUN	*Log all points in alarm from group upon alarm transition within group*
CLEAR LOG # POINT ALARM #-# ALARM POINT RUN	*same as:* CLEAR LOG # POINT #–# ALARM POINT RUN
CLEAR LOG # POINT ALARM #–# CLOCK # RUN	*Periodic log of points from group in alarm or having made a transition since last log*

ALARM RELAYS (requires Option A and ARP1)

CLEAR PRGM POINT #–# ALARM FUNC # – # – # – # RUN	*Assigns relays to point group (up to 4 per point)*
CLEAR PRGM ALARM FUNC #–# HI RUN	*Sets relay group on (high)*
CLEAR PRGM ALARM FUNC #–# LO RUN	*Sets relay group off (low)*
CLEAR PRGM ALARM FUNC #–# HI LO RUN	*Sets relay group flashing*
CLEAR PRGM ALARM FUNC #–# RUN	*Reset relay group to normally active status*
CLEAR LIST # ALARM FUNC #–# RUN	*List relay group status*
CLEAR DISPLAY ALARM FUNC #–# RUN	*Display relay group status*

DIGITAL INPUTS (requires Option D and Option M)

CLEAR PRGM FUNC 102 – # RUN	*Set digital option to # digit input (# = 2, 4, or 6)*
CLEAR RESET FUNC 102 – RUN	*Resets digital option, cancels points 101 and up*

STATUS INPUTS (requires Option D and Option M)

CLEAR LOG # FUNC 103 LO RUN	*Logs status change (low speed)*
CLEAR RESET FUNC 103 LO RUN	*Aborts low speed status scan*

PREFACE

The Digitrend 235 Maintenance Manual is supplied with each Digitrend 235 and contains technical information for assisting the user in servicing the instrument. The Digitrend 235 Maintenance Manual is written for the electronic technician level of experience. Effective usage of this manual requires that the reader be familiar with standard troubleshooting techniques and be able to perform a diagnostic analysis while referring to schematics, assembly drawings, and block diagrams. This manual contains four sections:

Section 1 - Calibration
Section 2 - Theory of Operation
Section 3 - Troubleshooting
Section 4 - Drawings and Parts List

Space is provided in the Maintenance Manual to insert an extra copy of the Digitrend 235 Operator's Manual.

Faulty circuit boards or the entire instrument may be shipped to Doric's Customer Service Department for repair. Documentation accompanying the board or instrument should include model number, serial number, your name, telephone number, and a brief description of the problem or rework instructions. The Customer Service Department may be contacted by phone to answer any questions related to a maintenance or service problem: Call (714) 565-4415 in California, or toll free (800) 854-2708 outside California.

Parts may be ordered from the factory. All correspondence for parts should be directed to the attention of Doric's Marketing Services department. A minimum order of $25.00 will be accepted on all orders for parts. A parts list for each Digitrend 235 printed circuit board assembly is found in Section 4 of this manual. Parts are ordered by part number, listed in the "drawing no." column on the parts list.

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TABLE OF CONTENTS

Section	Title	Page
LIST OF ILLUSTRATIONS		ii
SECTION 1 - CALIBRATION		
1.1	Calibration, General	1-1
1.2	Solid-state and Reed FEM Calibration	1-1
1.2.1	Preliminary Set-up	1-1
1.2.2	Calibration	1-2
1.3	Current FEM Calibration	1-5
1.3.1	Preliminary Set-up	1-5
1.3.2	Calibration	1-6
1.4	High Voltage FEM Calibration	1-8
1.4.1	Preliminary Set-up	1-8
1.4.2	Calibration	1-8
SECTION 2 - THEORY OF OPERATION		
2.1	Introduction to the Theory of Operation	2-1
2.2	Main System Boards, General	2-1
2.2.1	CPU Board Assembly, General	2-2
2.2.2	PIA Board, General	2-8
2.2.3	Front Panel Board, General	2-12
2.2.4	Power Supply Module, General	2-14
2.3	Front End Module (FEM), General	2-19
2.3.1	Analog Conversion Circuits	2-19
2.3.2	Solid-state Multiplexer	2-22
2.3.3	Reed Relay Multiplexer	2-23
2.3.4	RTD Multiplexer	2-23
2.3.5	Digital Communication	2-25
2.3.6	FEM Timing	2-30
2.3.7	System Algorithm	2-33
2.4	Option Board Assemblies, General	2-34
2.4.1	Memory Extension Board Assembly, General	2-34
2.4.2	Alarm Monitoring Board, General	2-39
2.4.3	Alarm Relay Panel, General	2-45
2.4.4	Serial I/O Port #2 Board, General	2-48
2.4.5	Digital Inputs Board, General General	2-53
SECTION 3 - TROUBLESHOOTING		
3.1	General	3-1
3.2	Preliminary Troubleshooting	3-1
3.3	System Support Tree	3-1
3.3.1	Power Supply Troubleshooting	3-2
3.3.2	CPU Board Troubleshooting	3-4
3.3.3	PIA Board Troubleshooting	3-4
SECTION 4 - DRAWINGS AND PARTS LISTS		
4.1	General	4-1

LIST OF ILLUSTRATIONS

Number	Title	Page
2-2.	Block Diagram, Solid-state FEM	2-20
2-3.	Integrator Output	2-22
2-4.	Block Diagram, Reed Relay Multiplexer	2-23
2-5.	Three-wire RTD Configuration, One Channel	2-24
2-6.	RTD Multiplexer Current Generator Switching	2-25
2-7.	Block Diagram, Data Receive/Decode Circuits	2-26
2-8.	Block Diagram, Data Shift/Encode Circuits (PIA)	2-28
2-9.	Timing Diagram, Data Encoding for Serial Transmission	2-29
2-10.	Mainframe Transmitter/Receiver Pair	2-29
2-11.	Timing Diagram, Basic Conversion Cycle	2-30
2-12.	Timing Diagram, Point Scanning Sequence	2-31

SECTION 1
CALIBRATION

1.1 CALIBRATION, GENERAL

The design of the Digitrend 235 incorporates digital data comparison that enables calibration of the FEM (Front End Module) from the front panel keyboard (digital calibration).

Digital calibration is implemented by entering the calibration voltage input value via the front panel keyboard. The entered number is compared to the actual reading and a ratio is computed which is stored in memory as a calibration constant.

Two calibration constants are stored in memory; referred to as the zero (offset) and +full scale (scale factor) calibration constants. The zero calibration constant is subtracted from the reading to set the zero reference point. The reading is then multiplied by the +full scale calibration constant to normalize the slope from the zero reference point.

Calibration is performed on the linear voltage functions of the FEM using one data point within that FEM. Solid State and Reed FEMs are calibrated to store the correct calibration constants for Functions 2, 3, 4, and 5. Calibration constants for High Voltage and Current FEMs are determined on Functions 6 and 4 respectively. When a FEM has been calibrated on one data point for the linear voltage functions, the FEM is calibrated for all data points and all functions.

An RTD FEM uses an onboard precision resistor (0.01%) for self-calibration. The resistor value is read periodically and the calibration constant updated. Therefore, no field calibration is required.

If a FEM is moved to a different slot location, re-calibration is required unless 0.2% accuracy is sufficient.

1.2 SOLID-STATE AND REED RELAY FEM CALIBRATION

Test Equipment Required:

Millivolt, volt, and current calibrator:
resolution, 1 uV; accuracy +/- .01% (+/- 2 uV).
Doric Scientific DS-808 or equivalent.

1.2.1 Preliminary Set-up

a. Apply power to the calibrator and allow warm-up time in accordance with the calibrator operating manual.

b. Adjust calibrator output to 0 (zero) volts.

c. Remove power from the Digitrend 235.

d. Remove the grounding lug from the FEM module to be calibrated; pull the FEM out of the chassis using the finger pull provided at the top of the module.

e. Set the module on a flat work area with the large bare aluminum plate on the module facing downwards. Remove the termination block cover by extracting the two philips head screws.

f. Buss all positive (+) inputs together and connect to the calibrator positive (+) output.

g. Buss all negative (-) inputs together and connect to the calibrator negative (-) output.

h. Replace the cover over the input strips.

i. Return the FEM to the chassis connector in which it will finally be installed.

j. Fasten the grounding lug at the bottom of the FEM module.

k. Apply power to the Digitrend 235, placing the key switch in PRGM, and allow 5 minutes warm-up time before proceeding to 1.2.2.a.

1.2.2 Calibration

a. Place the front panel key switch in PRGM if not already done.

b. Assign one of four linear voltage functions to all points within the FEM:

[CLEAR] [PRGM] [POINT] [first point no.] [-] [last point no.] [FUNC]

[function no.] [RUN]

The first and last points of the FEM are specified in accordance to the FEM slot location. Refer to Table 1-1 below.

TABLE 1-1. FEM POINTS VERSUS SLOT LOCATION

FEM SLOT	FEM FIRST POINT	FEM LAST POINT
1	81	100
2	61	80
3	41	60
4	21	40
5	1	20

Calibration is performed on each of these function numbers for Solid-State and Reed FEMs:

Function 2*
Function 3
Function 4
Function 5

*The lower range is specified as [1] if configuration switch #1 is open (low sensitivity) or [2] if configuration switch #1 is closed (high sensitivity). Refer to 4.5.3 in the Digitrend 235 Operator's Manual for more information on assigning function numbers to data points.

c. Adjust calibrator output to 0.000 mV (use lowest range).

d. Wait at least 10 seconds to allow all FEM channels to be read.

e. Log the points within the FEM:

[CLEAR] [LOG] [POINT] [first point no.] [-] [last point no.] [RUN]

f. Examine the log and determine which point number has its value closest to mid-point of the voltage scatter.

g. Access the point number determined to be at mid-point for calibration:

[CLEAR] [CALIB] [POINT] [point no. determined] [RUN]

The point number accessed for calibration will display its value on the seven segment LED display.

NOTE

Do not leave the Reed FEM in the calibration mode for more time than is necessary to perform calibration (approx. 20 seconds). Thermal offsets produced by the relay coil may introduce an error in calibration when time in calibration is in excess of 20 seconds.

h. Initiate the zero calibration constant computation by entering the following command sequence:

[CLEAR] [PRGM] [CALIB] [0] [RUN]

After entering the command sequence, the display will update with the correct reading of the input.

i. Exit the calibration mode by displaying the point or specifically aborting the calibration mode:

[CLEAR] [DISPLAY] [POINT] [point no.] [RUN]

or

[CLEAR] [RESET] [CALIB] [RUN]

j. Adjust the calibrator output to the +full scale value of the function being calibrated. Refer to Table 1-2 below.

TABLE 1-2. CALIBRATION TABLE FOR SOLID-STATE AND REED FEMS

FUNCTION	CALIBRATION VOLTAGE (+Full Scale)	KEYBOARD ENTRY*	COMMENT
1	+9.9900 mV	19980	Keyboard entry is 20% of input.
2	+20.000 mV	20000	
3	+80.000 mV	40000	Keyboard entry is 50% of input.
4	+400.00 mV	40000	
5	+2.0000 V	20000	

* For calibration of low sensitivity instruments, delete the last zero of the keyboard entries shown.

k. Wait at least 10 seconds to allow all FEM channels to be read.

l. Access the point used previously for calibration:

[CLEAR] [CALIB] [POINT] [point no. determined] [RUN]

The point number accessed for calibration will display its value on the seven segment LED display.

m. Initiate the +full scale calibration constant computation by entering the following command sequence:

[CLEAR] [PRGM] [CALIB] [+full scale value] [RUN]

After entering the command sequence, the display will update with the correct reading.

NOTE

Calibration of Function 1 requires that 20% of the +full scale value be entered when initiating the +full scale calibration constant computation. Calibration of Function 3 requires that 50% of the +full scale value be entered when initiating the +full scale calibration constant computation. Refer to Table 1-2.

n. Exit the calibration mode by displaying the point or specifically aborting the calibration mode:

[CLEAR] [DISPLAY] [POINT] [point no.] [RUN]

or

[CLEAR] [RESET] [CALIB] [RUN]

o. Repeat steps 1.2.2.b through 1.2.2.n for the remaining linear voltage functions to be calibrated.

SOLID-STATE AND REED FEM CALIBRATION COMPLETED

1.3 CURRENT FEM CALIBRATION

Test Equipment Required:

Millivolt, volt and current calibrator:
resolution, 1 uV; accuracy +/- .01% (+/- 2 uV). Doric Scientific DS-808 or equivalent.

1.3.1 Preliminary Set-up

a. Apply power to the calibrator and allow warm-up time in accordance with the calibrator operating manual.

b. Adjust calibrator output to 0 (zero) milliamps.

c. Remove power from the Digitrend 235.

d. Remove the grounding lug from the FEM module to be calibrated; pull the FEM out of the chassis using the finger pull provided at the top of the module.

e. Set the module on a flat work area with the large bare aluminum plate on the module facing downwards. Remove the termination block cover by extracting the two philips head screws.

f. Buss all inputs in series. The positive (+) input from Point 1 is connected to the calibrator positive (+) output. The negative (-) input from Point 1 is connected to the positive input of Point 2 with the negative input from

Point 2 connected to the positive input of Point 3 etc; continuing through all points in sequence, until the negative input from Point 20 is reached. The negative input from Point 20 is then connected to the negative output of the calibrator.

g. Replace the cover over the input strips.

h. Return the FEM to the chassis connector in which it will finally be installed.

i. Fasten the grounding lug at the bottom of the FEM module.

j. Apply power to the Digitrend 235, placing the key switch in PRGM, and allow 5 minutes warm-up time before proceeding to 1.3.2.

1.3.2 Calibration

a. Place the front panel key switch in PRGM if not already done.

b. Assign Function 4 to all points within the FEM:

[CLEAR] [PRGM] [POINT] [first point no.] [-] [last point no.]

[FUNC] [4] [RUN]

The first and last points of the FEM are specified in accordance to the FEM slot location. Refer to Table 1-1.

c. Adjust calibrator output to 0.0 mA.

d. Wait at least 10 seconds to allow all FEM channels to be read.

e. Log the points within the FEM:

[CLEAR] [LOG] [POINT] [first point no.] [-] [last point no.] [RUN]

f. Examine the log and determine which point number has its value closest to mid-point of the voltage scatter.

g. Access the point number determined to be at mid-point for calibration:

[CLEAR] [CALIB] [POINT] [point no. determined] [RUN]

The point number accessed for calibration will display its value on the seven segment LED display.

NOTE

Do not leave the Current FEM in the calibration mode for more time than is necessary to perform calibration (approx. 20 seconds). Thermal offsets produced by the relay coil may introduce an error in calibration when time in calibration is in excess of 20 seconds.

h. Initiate the zero calibration constant computation by entering the following command sequence:

[CLEAR] [PRGM] [CALIB] [0] [RUN]

After entering the command sequence, the display will update with the correct reading of the input.

i. Exit the calibration mode by displying the point or specifically aborting the calibration mode:

[CLEAR] [DISPLAY] [POINT] [point no.] [RUN]

or

[CLEAR] [RESET] [CALIB] [RUN]

j. Adjust calibrator output to 20 mA.

k. Wait at least 10 seconds to allow all FEM channels to be read.

l. Access the point used previously for calibration:

[CLEAR] [CALIB] [POINT] [point no. determined] [RUN]

The point number accessed for calibration will display its value on the seven segment LED display.

m. Initiate the full scale calibration constant computation by entering the following command sequence:

[CLEAR] [PRGM] [CALIB] [40000]* [RUN]

* For low sensitivity instruments (Configuration Switch #1 closed), enter [4000].

After entering the command sequence, the display will update with the correct reading.

n. Exit the calibration mode by displaying the point or specifically aborting the calibration mode:

[CLEAR] [DISPLAY] [POINT] [point no.] [RUN]

or

[CLEAR] [RESET] [CALIB] [RUN]

CURRENT FEM CALIBRATION COMPLETED

1.4 HIGH VOLTAGE FEM CALIBRATION

Test Equipment Required:

Precision Voltage Source:
resolution, 1 mV; accuracy +/- .01% Power Designs 2005A or equivalent

1.4.1 Preliminary Set-up

a. Perform preliminary set-up per steps 1.2.1.a to 1.2.1.j.

b. Apply power to the Digitrend 235, placing the key switch in PRGM, and allow 5 minutes warm-up time before proceeding to 1.4.2.

1.4.2 Calibration

a. Place the front panel key switch in PRGM if not already done.

b. Assign Function 6 to all points within the FEM:

[CLEAR] [PRGM] [POINT] [first point no.] [-] [last point no.] [FUNC]

[6] [RUN]

The first and last points of the FEM are specified in accordance to the FEM slot location. Refer to Table 1-1.

c. Adjust calibrator output to 00.000 volts.

d. Wait at least 10 seconds to allow all FEM channels to be read.

e. Log the points within the FEM:

[CLEAR] [LOG] [POINT] [first point no.] [-] [last point no.] [RUN]

f. Examine the log. If the voltage scatter of point values is less than 1 millivolt, calibration of the High Voltage FEM is not required. If the voltage scatter is greater than 1 millivolt, determine which point number has its value closest to the mid-point voltage scatter and proceed to the next step.

g. Access the point number determined to be at mid-point for calibration:

[CLEAR] [CALIB] [POINT] [point no. determined] [RUN]

The point number accessed for calibration will display its value on the seven segment LED display.

NOTE

Do not leave the High Voltage FEM in the calibration mode for more time than is necessary to perform calibration (approx. 20 seconds). Thermal offsets produced by the relay coil may introduce an error in calibration when time in calibration is in excess of 20 seconds.

h. Initiate the zero calibration constant computation by entering the following command sequence:

[CLEAR] [PRGM] [CALIB] [0] [RUN]

After entering the command sequence, the display will update with the correct reading of the input.

i. Exit the calibration mode by displaying the point or specifically aborting the calibration mode:

[CLEAR] [DISPLAY] [POINT] [point no.] [RUN]

or

[CLEAR] [RESET] [CALIB] [RUN]

j. Adjust the calibrator output to 22.000 volts.

k. Wait at least 10 seconds to allow all FEM channels to be read.

l. Access the point used previously for calibration:

[CLEAR] [CALIB] [POINT] [point no. determined] [RUN]

m. Initiate the +full scale calibration constant computation by entering the following command sequence:

[CLEAR] [PRGM] [CALIB] [22000]* [RUN]

* For low sensitivity instruments (Configuration Switch #1 closed), enter [2200].

After entering the command sequence, the display will update with the correct reading.

n. Exit the calibration mode by displaying the point or specifically aborting the calibration mode:

[CLEAR] [DISPLAY] [POINT] [point no.] [RUN]

or

[CLEAR] [RESET] [CALIB] [RUN]

HIGH VOLTAGE FEM CALIBRATION COMPLETED

SECTION 2
THEORY OF OPERATION

2.1 INTRODUCTION TO THE THEORY OF OPERATION

This section of the manual covers the theory of operation for each of the circuit boards in the Digitrend 235. Refer to the pertinent schematic in Section 4 when reading the theory for each circuit board assembly.

The theory of operation is divided into three major groups of circuit boards: (a) main system boards, (b) FEM analog sub-system, and (c) optional plug-in printed circuit board assemblies.

2.2 MAIN SYSTEM BOARDS, GENERAL

The following printed circuit board assemblies comprise the main system boards:

1. Central Processor Unit (CPU) board
2. Peripheral Interface Adaptor (PIA) board
3. Front Panel board
4. Power Supply Module

The main system boards controls and supports all functions required by the data logger.

The CPU board is the functional brain of the Digitrend 235 and is based on the 68B00 microprocessor. This board contains a crystal controlled master clock, most of system memory, and a serial I/O port. The CPU board interfaces to the rest of the system through the system bus, executing the program which forms the basis for all decision making processes, providing system timing and control signals, and monitoring system operation.

The PIA board interfaces the FEM and Front Panel board to the CPU board via the system bus.

The Front Panel board provides the man/machine interface for the Digitrend 235. The seven segment LED, status LED indicators, and audible beeper are driven by this board. Additional functions are performed by the keyboard decoding circuitry and the thermal printer control/driver circuitry.

The power supply module provides regulated power to all circuits in the Digitrend 235. Overvoltage and short circuit protection are incorporated.

The Main System boards are capable of operation as an independent unit. It can be programmed and operated in most modes without FEMs or option boards, for programming, testing, and maintenance.

2.2.1 CPU Board Assembly, General

Assembly: 231-4340-00
Schematic: 231-6340-00

The Digitrend 235 is based on the 68B00 microprocessor. It can be viewed as any other computer system that consists of a central processor unit (CPU), memory, and input/output (I/O) interface(s). The CPU board itself comprises a large part of the system. The CPU, most of system memory, and a serial I/O port are located on the Digitrend 235 CPU board.

The 68B00 microprocessor is both the heart and brain of the system. To ensure reliable operation of the microprocessor, it is fully isolated from all system signal lines by buffers and latches.

External memory (used for options and other ancillary functions) and other input/output devices in the system are accessed by the CPU through the Motherboard.

2.2.1.1 CPU Clock Generator

The CPU is driven by a two-phase non-overlapping clock consisting of crystal oscillator Y2, synchronous 4-bit counter 5P, and quad NANDs 3P and 4P.

Crystal oscillator Y2 provides the clock input (7.86432 MHz) for counter 5P, pin 2. The counter divides the input frequency by eight (C output 5P, pin 12) which provides the input for the R/S flip-flop circuit composed of NAND gates 4Pa and 4Pb. Toggling action is provided by NAND 4Pd used as an inverter across the inputs to the R/S flip-flop circuit (4Pb pin 4, 4Pa pin 2). The inverter causes the flip-flop to "set" and "reset" every time the output from counter 5P, pin 12, changes state. The output of the R/S flip-flop is buffered to the required levels by NANDs 3Pa and 3Pb, providing the 68B00 phasel and phase 2 inputs via the resistor network which is used to minimize overshoot and undershoot.

The propagation delay time of the R/S flip-flop prevents overlap between the falling edge of one phase and the rising edge of the alternate phase.

2.2.1.2 EXRAID Operation

The Digitrend 235 CPU board has a unique external raid feature that reverses the direction of the CPU board address and data buffers, and isolates the on-board microprocessor. This exraid mode causes the CPU board to appear as a memory and I/O board to the Motherboard bus.

In the exraid configuration, an external processor may gain access to the internal CPU bus for diagnostics, without removing the CPU board for reprogramming, or the need to halt the CPU to examine run-time variables at random execution times.

The data buffers reverse sense of direction and activation-decoding, thereby supporting an external device by allowing incoming signals to be decoded as though they originated with the host microprocessor.

2.2.1.3 Process Control Latches

The process control lines to the microprocessor, NMI, IRQ, and HALT, are latched on each cycle prior to entering the processor. This latching occurs on the falling edge of the UBF1 cycle to guarantee timing of the signals to the microprocessor. Latching the signals minimizes noise susceptibility. Clearing them on reset prevents ambiguous commands to the processor during resets.

2.2.1.4 Address/Control Buffers

Tri-state buffers are used to buffer the CPU clock, VMA, R/(not)W address lines A0-A15, and data lines D0-D7. This prevents excessive loading on the system bus, and also allows an external processor to control the system bus in lieu of the onboard microprocessor. On the schematic, these buffered lines are prefixed with "B" (i.e. BVMA is buffered VMA). Prior to buffering, each control line is gated to allow the watchdog circuitry to disable any attempted access to write-protected RAM (wpr), or open RAM (if reset is to be asserted).

The CPU clock (phase1) is buffered by gated buffer 2N (BF1, buffered phase1). R/(not)W and ERW(not) are ORed (1Gd), inverted (1Fc), and buffered/gated (2Na) to form BR/(not)W. Data lines D0-D7 are double buffered by data buffers 3K and 1A. Buffer 3K handles data to and from onboard memory (BD0-BD7). Buffer 1A handles data to and from external devices (D0-D7); however, the data exchange between the CPU and external devices requires that the data also pass through buffer 3K, resulting in double buffered data (BBD0-BBD7). Also refer to 2.2.1.11 and 2.2.1.12.

Address lines A0-A15 are also double buffered. Address buffers 3M and 4M are used to buffer the CPU address lines to onboard memory (4B-4G and 4H-4L), decoders (3G and 3H), and various gates. Connector address buffers 2A and 3A buffer the buffered address lines to external devices connected to connector P1 (A0-A15). The connector address buffers are used to isolate the CPU board internal address bus, BA0-BA15, from the Motherboard address bus, A0-A15, and to increase the drive capability onto the bus.

When the BEXRAID line is in the low state, buffers 2A and 3A route the internal BAxx lines onto the Motherboard. When the BEXRAID line is high, the buffers change direction, and drive the address lines from the Motherboard onto the internal address lines.

The uVMA (microprocessor VMA) line, EVMA (enable VMA), and RESET are NANDed together (NAND gate 3Ja) and buffered/gated to form BVMA(not). These circuits form BVMA(not) in normal operation of the system via the BEXRAID gate input on buffer 2Nc, pin 1.

The BEXRAID line is the CPU board control for direction of address/data signal flow. When the onboard microprocessor controls the system bus, BEXRAID is low and address/data flow is from the CPU to the Motherboard. This condition enables buffer 2Nc to pass the NANDed uVMA, EVMA, and RESET as BVMA(not). Conversely, BEXRAID(not) is high, holding buffer 2Nd in tri-state, which prevents VMA(not) from being output as BVMA(not).

When the system bus is relinquished to an external processor (EXRAID mode), BEXRAID becomes high and address/data flow is from the Motherboard to the CPU board. This condition tri-states buffer 2Nc and enables buffer 2Nd to pass VMA(not) as BVMA(not).

2.2.1.5 ROM

ROM consists of four 8K x 8 masked ROMs (4I-4L) and one 2K x 8 patch ROM (4H).

Basic ROM decoding originates from PROM 3H (512 x 8). The high to low address lines of the ROM are driven from BA14 to BA6, respectively. The eight outputs (3H pins 9-11 and 13-17) form inputs to gates to qualify ROM selection. In addition, outputs PA6-PA10 form the higher order address for Patch ROM 4H when that ROM is enabled. A particular ROM is selected by lines PE0(not) through PE3(not). The Patch ROM is selected by RPE(not). Selection is accomplished via NANDs 3Ia-3Ic, 3Jb, and 3Jc.

PA6-PA10 are used as either ROM select signals, or as higher order address for Patch ROM 4H depending on the states of 3H pins 16 and 17.

Three qualifiers are needed to select a particular ROM; representing the three inputs to a particular NAND controlling that ROM. The selection of ROMs 4I-4L is performed as follows:

The first qualifying function is performed by NOR 2Ic. The output of NOR 2Ic must be high to select a ROM. This would require, first, that BA15 and BVMA be high, which is then NANDed by 2Jc providing a low on NOR 2Ic, pin 8; and secondly, the output at 3H, pin 17, be driven low providing a low on NOR 2Ic, pin 9. With pin 17 low, PA6-PA9 is used for ROM selection (second qualifier). If pin 17 is high, PA6-PA10 is used for higher order address for Patch ROM 4H.

The second qualifying function is performed by PROM 3H, output lines PA6-PA9. Since these lines are normally pulled up to +5 volts via RN6, ROM 3H deselects those lines whose NAND and therefore ROM, is not to be selected. The PROM will drive three of these four lines low. The line remaining at +5 volts qualifies that particular NAND.

The third qualifying function is the buffered phase1 clock (BF1). The clock synchronizes selection of ROM when the clock cycle is high.

When the inputs to a NAND are all high, the pertinent ROM is selected.

Selection of Patch ROM 4H is performed as follows:

PROM 3H decodes the address which selects and addresses the Patch ROM. When the Patch ROM is to be selected, PROM 3H pin 17, is driven high. This provides a high input to NAND 3Jb pin 5. In addition, BA15 and BVMA must both be high at 3Jb pins 3 and 4. When all of these conditions are met, the output of NAND 3Jb goes low which selects Patch ROM 4H. PA6-PA10 is then used for the higher order address for 4H.

The signal on 3H pin 16 selects ROM access onboard, or offboard. The ROM area is defined as A15&VMA. If pin 16 is low, onboard ROM is selected. If pin 16 is high, offboard ROM is selected.

The WRPTA(not) line (3H pin 15) selects protected or unprotected data zones in the lower 32K of memory in the Digitrend 235. This line is programmable high or low for 64 byte sections of memory on 64 byte boundries. When this line is low, the memory location being accessed is a write protected location, and must be opened by toggling the write protect line on the PIA card high prior to writing. When WRPTA(not) is high then the accessed location is not write protected.

2.2.1.6 RAM

The RAM area is composed of CMOS, battery backed-up RAM chips 4B, 4C, 4D, 4E, 4F, and 4G (each 1K x 4). It is organized as 3K of contiguous memory, starting at 0000hex, and running through 0BFFhex.

RAM and peripheral decoding is performed by decoder 3G. This chip is enabled when pins 4 and 5 are low, and pin 6 high. The address lines BA10-BA12 are decoded by 3G, and gated with BA13 (2G) and BF1 (2F) to force one of four lines low: PER1(not), RE0(not), RE1(not), and RE2(not). RE0(not) through RE2(not) controls the RAM chip enables on 4B-4G, via transistors Q9-Q11. PER1(not) is used to select PIAs on the PIA board assembly and the ACIA on the CPU board assembly.

RAM selection is done in pairs. For example, RAM 4B and 4C are enabled when RE0(not) goes low. This is accomplished by driving BRE0(not) low via transistor Q9. Normally, BRE0(not) through BRE2(not) is held high to Vbb by pull-up resistors R33-R35. RC networks composed of RN4 and C9-C11 filters potential noise resulting from the transitions. Each RAM pair selection represents 1K of RAM space:

00 = 0000-03FFhex
01 = 0400-07FFhex
02 = 0800-08FFhex

RAM accesses are synched to the BF1 line from the microprocessor which ensures clean latching of the address bus (since the RAMs latch address internally), and providing at least 20ns of data hold time from the deselection of RAM.

Peripheral space uses Y0 and A13 high (2000-23FFhex) to achieve 22xx hex for peripheral decoding (A9 is used at each device for decoding); this is the PER1(not) line.

Q8, RN4 and RN5 form the RAM reset disable circuitry. This circuit assures that the RAMs remain disabled (chip enables at Vbb) when system voltage falls low, or upon resets.

2.2.1.7 RAM Battery Back-up System

CPU RAM memory is provided with battery back-up cicuitry comprised of Q4, Q5, BT1, R16, R17, S1, and C6. In normal operation, Q4 is forward biased by +5 V at the emitter, which supplies a trickle charge to BT1 via resistor R16, and providing Vbb for RAM memory from the collector. Vbb tracks the +5 volt bus until the voltage drops below 2.4 volts; thereafter, Vbb is held at +2.4 volts via transistor Q5 and battery BT1. Since Q4 is reversed biased by the battery voltage with the emitter below +2.4 volts, battery back-up is confined to the Vbb bus. C6 decouples any transient noise to ground. S1 is used to clear the RAM memory by removing the battery voltage from the Vbb bus.

2.2.1.8 Watchdog

The watchdog circuitry, 3N and 1H, is centered around the use of a dual-D flip-flop to detect the failure of the microprocessor to perform a write function in a given time period. The flip-flop forms a missing pulse detector for

uR/W, and a pulse-stretcher for the other error detection circuits.

When the write pulse stream is broken, or an alternate error circuit triggers, the two flip-flops latch up, requesting a reset, until the reset circuitry responds with reset going low, clearing the circuit.

Another input to the watchdog circuit is the forced failure line, RHLT(not), which will go low when a write to ROM (BVMA and BA15), or a write to protected RAM (WPR), occurs while write protect is in effect.

These conditions will produce disables to the gating for the BVMA and BR/(not)W control lines (preventing the microprocessor from disrupting memory), and will initiate a latching pulse to request reset from the write drop-out detect circuit.

2.2.1.9 +5 Volts Low Detect Circuit

The +5 Volts Low Detect circuit uses an LM393 op amp (1M) to compare the +5 volt bus, via R41, to a reference voltage from CR9. When the 5 volt line drops below about 4.75 volt, the comparator will swing low, triggering the halt reset sequencer. Potentiometer R41 is used to adjust the division ratio of the 5 volt line. This is compared to the voltage on CR9, an ICL8069 voltage reference. When the divided 5 volt level drops below the reference voltage, the op amp output swings negative, causing the second op amp to also swing negative. This forces the CPU into halt, and activates the reset circuit. R37 and C12 act as a filter for the 5 volt line, and R45 increases the hysteresis of the detector. C15 and C16 provide line filtering.

2.2.1.10 Remote Start

The remote start circuit resides at 2240hex. It provides an interrupt if a switch closure occurs on either, or both, inputs. When the CPU receives an interrupt on either line, it will read address 2240hex. It may find that D7 is low from a closure on input 2, or D6 is low from a closure on input 1. The interrupt and the logic lows may be cleared by writing any number to 2240hex.

In this circuit, the closure of a contact shuts off an opto-isolator (1B), causing a rising edge to the clock input of the corresponding flip-flop (1Ca and 1Cb). The rising clock edge causes the flip-flop to latch a low from the D input tied to ground. The Q output is then inputed to its gated data buffer (1Db and 1Dc).

The complement output from the flip-flop (Qnot) then turns on transistor Q12, which drives IRQ(not) low, posting an interrupt to the microprocessor. Reading the remote start port turns on these buffers. Writing to the port forces a preset of both flip-flops, and removes the posted interrupt.

2.2.1.11 Data Buffers

There are two data buffers on the CPU board. Data buffer 3K separates the microprocessor section (BBDx) from the memory section (BDx). Data buffer 1A separates the memory section (BDx) from the Motherboard connector (Dx).

The logic states of IIO (internal I/O) and BEXRAID enables or disables CPU to memory buffer 3K via exclusive OR 1Jd. With BEXRAID low (normal system opera-

tion), buffer 3K is disabled by IIO high when the CPU is accessing one of the devices on the internal data buss (BBDx). This serves to isolate the internal data from the onboard memory and external devices. When the CPU accesses its onboard memory, or any offboard device, buffer 3K is enabled by IIO low.

Buffer 1A is disabled by EDB(not) high when the CPU accesses its onboard memory. This serves to isolate the data interchange between CPU and onboard memory from external devices. When the CPU accesses an offboard device, EDB(not) is low, enabling buffer 1A. EDB(not) is gated by BF1 using NAND 2Jd. This results in EDB(not) being low only when BF1 is high. Thus, buffer 1A is enabled only when BF1 is high and disabled at all other times.

All these states are valid for BEXRAID being low. When BEXRAID is high, the buffers are enabled when they would normally be disabled, thereby separating the memory section from the Motherboard data bus when in the EXRAID mode.

A special read/write line, SR/(not)W is created to determine the direction of data flow through the two data buffers. This signal is the BR/(not)W line, complemented, or not complemented, depending upon the state of the BEXRAID line. When BEXRAID is high, this line is the complement of the BR/(not)W line. When BEXRAID is low, this line is the same level as the BR/(not)W line.

When BEXRAID is low, a read from an external device device copies data from the Motherboard data bus, D0-D7, onto the CPU data bus, BD0-BD7. A write to an external device causes the CPU data bus to be copied onto the Motherboard data bus.

When BEXRAID is high, a read by an external device copies data from the CPU data bus onto the Motherboard data bus. A write by an external device causes the Motherboard data bus to be copied onto the CPU data bus.

2.2.1.12 Serial I/O Port

The CPU board serial interface uses a 6850 ACIA for serial communication. The ACIA is programmable from the data bus for either 7-bit or 8-bit communication, with or without even or odd parity, and with variable stop bits. The microprocessor programs the control port of the ACIA for the mode of transmission, and monitors the control port for received data or empty transmitter port flags. The data is received and read through the data port, and is transmitted through a write to the data port. For the CPU board ACIA, the data port is at 2221hex, and the control port is at 2220hex.

The serial transmitted and received data, and additional control handshake lines are buffered for driving the serial link lines prior to the connector. The serial output data drives both the RS-232 driver and 20 mA current loop driver at the same time.

The control lines are all received and buffered as RS-232 levels, and are all pulled onboard to the inactive state. The incoming serial data from the RS-232 and 20 ma current loop are ORed together with the assumption that one of the lines will always be in the inactive state when the alternate line is being used. To meet RS-232 standards, the RS-232 serial input line must be taken to the inactive state externally when using the 20 ma current loop input.

The 20 ma current loop mode of transmission and reception uses a current-limiter circuit to drive an opto-isolator. The current-limiter circuit is front-ended with a full-wave rectifier, which depolarizes the incoming drive current to the circuit.

Current loop communication may be operated in the passive mode (the external device provides the 20 ma current source), or in the active mode (the Digitrend 235 power supply provides the 20 ma current source).

The baud rate for the serial I/O is established by bit rate generator 1R. Crystal Y1 (1.8432 Mhz) establishes the clock source for 1R. Frequency outputs 1R pins 1-3, 7, 9, and 13 are 16 times the data rate and is input to ACIA 2L, pins 3 and 4, via switch assembly S3. Data is synchronized internally by 2L with a clock rate 16 times the data rate. This provides a divide-by-16 clock ratio for internal synchronization. Since the transmit and receive clock inputs are tied together on ACIA 2L pins 3 and 4, transmitting and receiving is done at the same rate.

Since the baud rate is the reciprocal of the time for transmission of one bit, true data rate for transfer depends upon the number of bits per byte (including parity, start, and stop bits - up to 11 bits), and the true maximum data rate of the machine. With a fully loaded Digitrend 235, the throughput is approximately 240 bytes/second. At higher baud rates, this can appear as data bursts on a terminal, or at the host computer.

2.2.2 PIA Board, General

Assembly: 231-4310-00
Schematic: 231-6310-00

The PIA board interfaces the Front Panel board and FEM assemblies to the CPU. The PIA board uses three 6821 peripheral interface adapters for these tasks, two for the Front panel interface, and one for the FEM interface.

These adaptors allow interfacing of the external signals generated by the Front Panel board and FEM to the CPU as well as interfacing CPU signals to the external circuitry (Front Panel board and FEM).

The PIA board can be divided into seven functional sections:

1. FEM INTERFACE
2. BINARY COUNTERS
3. FEM INTERFACE CIRCUIT AND SERIAL ENCODER
4. WATCHDOG CIRCUIT
5. WRITE PROTECT HANDSHAKE CIRCUIT
6. DISPLAY PIA AND PRINTER PIA
7. DATA BUFFER ENABLE/DATA, ADDRESS, AND CONTROL BUFFERS

2.2.2.1 FEM Interface

PIA 4B provides the interface between the CPU and FEMs. Data from the CPU to the FEM consists of a 16-bit data stream which starts the FEM and PIA counters, initializes the FEM A/D converter, and provides configuration data to accomodate the data point being measured. Data from the FEM to the CPU consists of the latched count value from the PIA binary counters initiated by the zero cross detect pulse from the FEM, or detection of an over-range condition (input overload or broken thermocouple). FEM data is input/output on 4B pins 2-9 (peripheral data register A) and forms the basis for DATA BUS 2.

2.2.2.2 Binary Counters

The counter circuitry consists of two sequential binary counters, a high order counter and a low order counter (4F and 4C respectively). These counters, which are continuosly driven by the CPU phase1 clock (BF1), provides the raw counts which represents the FEM data point value when a zero cross is detected. The counters also provide the various signals (f6, f7, and f17) which modulate the FEM serial data from shift registers 5C and 5D for serial transmission to the FEM. The higher stages of the counter (lower frequencies) are reset from the system reset line (BRESET) to provide a minimum time from reset to the first post reset NMI. The lower stages of the counter are reset from a power supply sync circuit that synchronizes phase1 and phase2 from the power supply square wave output, with the CPU NMI. The power supply timing interface (phase1 and 2) is required for proper operation of the FEMs, as FEM timing is derived from this source.

2.2.2.3 FEM Transmit and Receive Interface

The CPU to FEM data is output from peripheral data register A (4B, pins 2-9). This data is sequentially output in two 8-bit bytes to shift registers 5C and 5D. The same data register is used to read the latched counter value from latches 4D and 4E when a zero cross, or an overload condition is detected. The output from these latches are read sequentially in two 8-bit bytes.

The gamma0 and gamma1 lines (4B, pins 16 and 17) are used to select which of the four registers (4D, 4E, 5C, and 5D) are to be active on DATA BUS 2.

CPU to FEM data is output as follows:

Gamma0 and gamma1 (4B pins 16 and 17 respectively) are NANDed (3Ca, 3Cd) with E0 (4B pin 19) to select the operating mode of shift registers 5C and 5D. When pin 9 of the shift register is high, the data on DATA BUS 2 is parallel loaded onto the shift register. When pin 9 of the shift register is low, data within the register is shifted synchronously with the positive transition of the clock. Shift register 5C is loaded with the FEM programming data. Shift register 5D is loaded with all "ones". When the correct data appears on the shift register inputs, the data is loaded in by a high on pin 9 of that register. When both registers are loaded, pin 9 of both registers goes low and the data is ready to be shifted for encoding.

The 15 Hz clock (f17) initiates the shifting/encoding sequence. When the 15 Hz clock is low, a high appears on the clock input of flip-flop 5Fb, clocking the state of the CLEAR input (which is high) onto the Q output. In addition, the high transition to the clock input is coupled by C1 and input to flip-flop 1Ab which drives the Q output low if no zero cross was detected. This causes counters 4E and 4D to latch the zero count (the instant f17 goes low, the counter stages revert to zero). The latched zero count is read into the PIA (E1 high) via DATA BUS 2 and interpreted as an over-range or broken thermocouple condition. Thus, the latch, read, and reset sequence is completed whether or not a zero cross pulse was received to initiate the sequence.

Flip-flop 5Fb is controlled by counter 1B and is used to enable NAND 3Fb utilized as a pulse gate. The pulse gate is enabled for the duration of 16 clock pulses (modulated data). Counter 1B counts the DATA 0 pulses. When 16 pulses are counted, 1B pin 5 (E2) outputs a high which resets 5Fb via

exclusive-OR 5Ea used as an inverter. This forces the output at 3Fb to remain high until E0 goes high (1B reset) and f17 goes low, whereupon another cycle of data shifting/encoding is begun.

The data shift/encode circuitry is comprised of flip-flop 5Fb, exclusive-OR 5Ea and 5Eb, inverter 1Ec, and counter 1B.

Data shifting/encoding is done as follows:

The data is input to 5Eb where it is exclusive-ORed with 15 kHz (f7). This results in the 15 kHz signal being modulated by the data. When the data appearing at 5Eb pin 5, is high, the output of 5Eb is 15 kHz out of phase with f7; when the data is low, the output is 15 kHz in phase with f7. The 15 kHz output from 5Eb is NANDed with 30 kHz (f6) which results in a 15 kHz output delayed by 1/2 cycle from the 15 kHz input and with 25% more duty time than the 15 kHz input. The net result is that the positive transitions of the modulated data occur mid-point of the 15 kHz state (f7) opposite the data. If the data is high, positive transitions of the modulated data (DATA 0) occur exactly mid-point of f7's low cycle. If the data is low, positive transitions of DATA 0 occur exactly mid-point of f7's high cycle. Whether the data is "one" or "zero" results in a positive transition from DATA 0 which serves to shift out the next bit from 5D pin 3. The FEM detects the logic level by comparing the positive transitions with the 15 kHz clock. When the positive transitions occur in relation to the clock determines the logic state.

Two multiplexed loops are used by the PIA card to serially transmit and receive FEM data.

DATA 0 is transmitted to the FEM by controlling a current loop consisting of multiplexer 2B, de-multiplexer 3B, and the FEM receive opto-coupler. Multiplexer 2B supplies the current source; de-multiplexer 3B supplies the current sink. DATA 0 turns on/off the current source/sink depending on the transitions made by DATA 0. The beta lines (beta0-beta2) are used to vector the FEM to which data is being transmit.

The FEM zero cross pulse is received by the PIA card on a loop consisting of multiplexers 2A, 3A, and the FEM transmit opto-coupler. Multiplexer 2A supplies the ground return for the FEM's opto-coupler transistor. Multiplexer 3A supplies the +5 volts pull-up for the FEM's opto-coupler open collector. The alpha lines (alpha0-alpha2) are used to vector the FEM from which the zero cross pulse is to be received.

The transmit/receive loops operate simultaneously; both addressing a different FEM sequentially in an interlaced manner. As one FEM is addressed for programming, another is being addressed for the zero cross pulse.

When the FEM detects a zero cross, a pulse is generated by the FEM which sinks the +5 volt pull-up (3A) to ground (2A) via the FEM's transmit opto-coupler. The resultant low appears on the D input of flip-flop 1Ab, and clocked in by f1 (1 Mhz), latching the Q output of 1Ab low via feedback resistor R7. The $\overline{Q}$ output is inverted by 1Eb, providing E3 which serves to latch the count value of 4F and 4C onto latches 4D and 4E. At the same time the Q output of 1Ab latches low, the Q(not) output goes high; inhibiting receive multiplexers 2A and 3A.

With the count value latched in, the two latches are then sequentially output onto DATA BUS 2 by inputing a low on the OE input one at a time. NANDs 3Cc and 3Cb control the OE inputs. E1 is an enable for OE, and gamma0 and gamma1 selects one of the two latches. After the contents of both latches are output on DATA BUS 2, the CPU converts the counts into a discrete point value.

2.2.2.4 Watchdog Circuit

The watchdog circuit is comprised of flip-flops 1Fa, 1Fb, and 2Eb; NANDs 3Ec, 3Ed, and 3F; NOR 2Fb; inverter 3Dd; and counter 2Db. This circuit alternately monitors the data being transmitted to the FEMs (CATCH1[not]), and the scan clock being transmitted to the front panel displays (CATCH2[not]) for any dropout in the signals. If a dropout occurs, a reset request (R REQ) is sent to the CPU.

The watchdog circuit also accepts the RES REQ line from PIA 2H, pin 17, via inverter 3Dd. This line allows the microprocessor to reset the system on power down, or if a failure is detected.

The R REQ signal, generated by the watchdog circuit, is sent to the CPU board to provide a system reset. The system reset (BRESET[not]) then clears the watchdog circuit.

2.2.2.5 Write Protect Handshake Circuit

The write protect handshake circuit is comprised of flip-flops 1Ca, 1Cb, 1Da, 2Da, 2Ea, and 1Db; NORs 2Fa and 2Fc; inverters 1Ee and 1Ef; and NANDs 3Eb and 3Fc.

When the CPU detects a write protected memory location, it transmits a WRPTA signal to the system. If the CPU has opened the WPR window by toggling the PRO REQ line high, the WPRO(not) line will be high, indicating a write to this location is legal.

If the WPRO(not) line is low when the CPU attempts to write to a WPR location, VMA is retracted, and R/W is taken to the read state (high), and the system is reset by the CPU board, indicating a write failure has occurrred.

When the CPU opens the WPRO(not) line, two types of counters are used to ensure the window does not malfunction. One counter consists of flip-flops 1Ca and 1Cb. These flip-flops advance the PRO REQ line to the reset of the WPRO(not) line, allowing WPRO(not) to be enabled for 500-700 microseconds only.

The second counter, consisting of flip-flops 1Da and 2Da, counts the number of writes to WPR memory, which serves to close the window after the third write. Therefore, the CPU may either write a byte of data, or an address (2 bytes) into memory with the WPRO window open. No more than three consecutive BF1 periods of write to protected memory are permitted. Thereafter, the window is closed, and must be reopened for further writes.

NAND 3Eb and flip-flop 2Ea inhibits the NMI line during WPRO(not) legal writes, to prevent NMIs from extending the WPR window beyond the defined time allocated to it.

Write protected RAM is used to store calibration data, alarm setpoints, back-up copies of the job tables, and system configuration data.

2.2.2.6 Display PIA and Printer PIA

In addition to the FEM PIA, two additional PIAs are used in the PIA card. One PIA (2H) controls the operation of the front panel keyboard/display/ buzzer circuits; the other (3H), the thermal printer circuits. The display PIA exists at four consecutive locations from 2208hex, and the printer PIA exists at four consecutive locations from 2210hex.

PIA 2H interfaces the CPU to the display LEDs, the keyboard decode matrix, the buzzer, and the write protect and reset request circuits. For display, the PAx lines are programmed as outputs; each output controlling one segment of the LED display, and input to the appropriate transistor driver on the Front Panel board. Scan clock toggles whenever the PAx lines are read, and scan reset is level programmed through the B side control register.

For the keyboard, the PB0-PB3 lines are programmed as inputs. PB4 is an input line for the key switch $\overline{\text{PRGM}}$ signal, and PB5-PB7 are output lines for BUZZ, PROREQ, and RESREQ. The buffered low line, BLOWL, is an edge triggered input to the PIA, which is used to signal the CPU that the power supply primary voltage is dropping low. The source for this signal originates from the power supply card.

For the printer, all port lines in PIA 3H are programmed as outputs. These outputs are routed to the printer via the Front Panel board drivers 2E, 3E, and 4E (refer to Front Panel board schematic 231-6320-00). The control lines are level outputs (CA2 and CB2), and edge triggered inputs (CA1 and CB1).

2.2.2.7 Address/Control and Data Buffers

All data and address lines on the PIA board are buffered by LS245 buffers, 4A and 5A, before entering the board.

Address buffer 5A (for addresses, F1, and PER1[not]) is always enabled to transmit into the PIA control bus 1.

Data buffer 4A is bi-directional, and is controlled by the buffered R/(not)W line and the enable data buffer (EDB[not]) line. The data buffer enable circuitry provides the EDB(not) line and is comprised of NANDs 1Ha and 3Ea; NOR 2Fd; and inverters 1Ed and 2Cd. All inputs to 1Ha must be high to enable data buffer 4A; as a result, the data buffer is enabled only during a high cycle of BF1. The R/(not)W line controls the direction of the data buffer, and is inverted by 2Cb to provide the DIR input for 4A. Inverter 2Cc inverts the inverted R/(not)W to provide BR/(not)W for use elsewhere on CONTROL BUS 1.

2.2.3 Front Panel Board, General

Assembly: 231-4320-00
Schematic: 231-6320-00

The Front Panel board provides the man/machine interface with the Digitrend 235. It contains the drivers for the LED display, encoding circuitry for the keyboard, drive circuitry for the audible beep, and control and drive circuitry for the printer head and motor. All Front Panel board circuits are under software control through the PIA board interface to the CPU.

The Front Panel board can be divided into four functional sections:

1. DISPLAY DRIVE CIRCUITS
2. PRINTER CONTROL CIRCUITS
3. RESET INTEGRATOR
4. BUZZER CIRCUIT

2.2.3.1 Display Drive Circuits

The display circuitry is arranged in a display matrix, using common segment lines (SEG A through SEG H), driven from PIA port A on the PIA board. A low on any of the common lines will enable a constant-current source, supplying 180 mA per segment. The segments are illuminated when the common cathode of the display is low; completing a path of conduction for the LEDs within that display.

The cathode of each display and LED (DS1-DS17) is connected to the output of two Darlingtons connected in parallel, using Darlington transistor arrays 1C and 1B. The parallel configuration provides higher load current capability. The Darlingtons sink the appropriate cathode when the input, controlled by Johnson counter 2C, is high. The buffered outputs of the Johnson counter (E0-E9) multiplexes the display and LED indicators by sinking the cathodes sequentially one at a time at the rate of the $\overline{\text{SCAN CLOCK}}$ input. The buffered outputs are also used for the decode scan of the keyboard and configuration diodes.

Configuration diodes are installed in spare slots in the keyboard matrix. These diodes are switched "in" or "out" by DIP switches S1-S3. As the matrix is scanned, a diode with an "on" switch will pull the associated line (E7-E9) high. These lines are buffered (2A), then returned to PIA 2H (on the PIA board) port B low order bits (KYBD0-KYBD3).

With each scan cycle, the display and keyboard inputs are strobed, and the configuration diodes are read and stored for interpretation.

The scan is reset by the SCAN RES line, and clocked by the SCAN CLOCK line; both originating from PIA 2H on the PIA board.

2.2.3.2 Printer Control Circuits

The thermal printer prints a line of 12 characters (max) wide in a 5 x 7 dot matrix. Each line is printed sub-column by sub-column (1-5) and sub-row by sub-row (1-7) on all 12 characters simultaneously until the entire line is printed.

Two one-shot timers on the Front Panel board are used to control the thermal printer.

One-shot 4Ab controls the burn-time of each sub-column. Transistors Q1, Q2, and associated circuitry are used to vary the charging rate of C2, which varies the pulse width of the Q(not) output, and hence, the burn-time. After receipt of the BURN START positive transition, 4Ab times out and BURN STOP is output, and a new sub-column is ready to be burned (printed). Johnson counter 4C sequentially burns each sub-column with the receipt of a BURN START input on the clock. The burn pattern for a particular character is determined by the COL1-COL12 lines originating from the printer PIA, and is taken from the resident program by the CPU.

One-shot 4Aa advances the printer motor one sub-row after a period of time determined by R1 and C1 has elapsed. The elapsed time is from the negative transition of DOT STEP, and provides sufficient time for the printer to print one entire sub-row 12 characters across before the next sub-row is to be printed. As the the motor is stepped to the next sub-row by DOT CLOCK, counter 4C is cleared, and each sub-column of the new sub-row is then sequentially burned. After all five sub-columns are burned, the process repeats itself until all

seven sub-rows have been processed, which completes the printed line. Thereafter, the motor steps a line space by several DOT STEP/DOT STOP cycles and a new line of information is begun.

2.2.3.2 Reset Integrator

System resets are of two types; power "on" reset, and system failure reset. The latter may originate from either a hardware failure, or a software error. The reset integrator (3B) counts failure resets, and stores this information for approximately 48 hours after the last failure reset.

On power up, all integrator flip-flops in 3B are cleared. Any reset after power up will cause a falling edge on the reset line, which will clock through the flip-flops via NOR 4Bd. The "zero" on the input of the shift register formed by these flip-flops will clock through to the successive stages with each reset pulse.

The first and third stages are connected to remove configuration diodes 11 and 12 on the respective post power up reset. The CPU monitors these diodes, and will output a "RESET" message after the first such reset. After the third reset, with both diodes now removed, the CPU will reset jobs (call original program information from protected RAM), and output a "RESET JOBS" message.

As the first RESET is detected, the TIME E(not) line goes low, and counters 3D and 3C start to count the number of display scans. When both counters overflow, reset integrator 3B will be automatically reset by OVEC. The counter period is approximately 48 hours. If no resets occur to reset the counter during any 48 hour period following the previous reset, the counter overflow will clear the reset integrator, clearing the system record of post power up resets.

2.2.3.4 Buzzer Cicuit

The buzzer circuit consists of a pair of one-shots (1E), transistor drivers (Q21, Q22), and a piezo-electric transducer (Y1). One-shot 1Ea is wired as a timer, to determine the duration of the buzzer. This one-shot is triggered by the falling edge of the BUZZ line from the display PIA on the PIA board.

One-shot 1Eb is triggered initially by the output of 1Ea. It then retriggers itself until 1Eb times out. This action creates a square-wave oscillation frequency of approximately 3 KHz. The Q and Q(not) outputs of 1Eb serve as base drives to drivers Q21 and Q22, which in turn energizes transducer Y1; producing the audible beep.

2.2.4 Power Supply Module, General

Assembly: 231-4500-00
Schematic: 231-6500-00

The power supply board supplies power to all circuits within the Digitrend 235. The line voltage is filtered for RFI rejection, rectified to give about 300 Vdc, and then reduced to about 116 Vdc by a switching regulator.

A power inverter, driven by a phase-locked oscillator, supplies two square-wave outputs that are rectified and filtered to give +5, +16, and -16 Vdc. Two regulated voltages of +12 and -12 Vdc are obtained from the +16 and -16 Vdc supplies, respectively.

The Power Supply can be divided into five functional sections:

1. INPUT CIRCUITS
2. SWITCHING REGULATOR
3. REGULATOR/CONTROLLER
4. OSCILLATOR, DRIVER, AND INVERTER
5. OUTPUT REGULATORS AND FILTERS

Each of these sections is described in the following paragraphs.

2.2.4.1 Input Circuits

A Pi filter is used in the high and low power leads to exclude RFI from the power supply input, and to prevent switching spikes from getting into the power leads.

A key-switch is used to turn the instrument on or off, or to put it in the program mode. In the latter case, a ground is placed on the PROGRAM line to P1 pin A, to output a low to the PIA PROG line.

The ac input is full-wave rectified by CR31 through CR34, then filtered by C26 and C27. Jumpers are inserted at the fuse block (as shown on the schematic) for 115 VAC operation, to form a voltage doubler network that supplies approximately 300-350 Vdc to the switching regulator.

For 230 VAC line operation, no jumpers are required. The 230 VAC line is full-wave rectified to again provide approximately 300-350 Vdc to the regulator.

Spark gaps SG1 and SG2 will arc over (and thereby blow the fuse) if more than about 470 volts is sent to the switching regulator. This prevents excessive line voltage from destroying the switching regulator.

2.2.4.2 Switching Regulator

The switching regulator reduces the unregulated 300 Vdc to a nominal 116 Vdc. The switcher is a free-running power oscillator that charges T3, a 3mh ferrite core inductor, then dumps the stored inductive energy into C7.

When Q16 turns on, the collector current ramps upwards until it reaches about 1.0 amp. At this point Q15 is turned on, which removes Q16's base drive (supplied by Q14). Q16 then shuts off, and CR45, R50 and C29 form a snubber circuit that absorbs some of Q16's switching energy and further turns on Q15 by increasing its base drive through R51. The collector-emitter voltage of Q16 rises until it is stopped by the "catch diode", CR44.

At this point, the inductor's voltage has gone from about +220 V to -116 V, and the inductor's current begins to ramp down towards zero. The average current through the inductor is about .5 A; thus, the maximum power transfer from the switching regulator is .5 A x 116 V = 58 watts. In practice it is actually less than this because there is a small amount of dead time between cycles.

The switching regulator would overcharge C7 if it was left to oscillate continuously. Instead, it is controlled by the regulator which shuts off the switcher by turning Q13 on. This holds off the base drive to Q16 and thus prevents it from turning on. R49, Q14 and CR42 provide a base drive circuit for Q16. When Q16 is on, the secondary of T3 puts out about 10 V. This turns Q14 on, which sources a heavy current into Q16's base, thereby holding Q16 on.

As Q16 begins to saturate (collector voltage equals base voltage), CR41 begins to conduct and this shunts the base current of Q16 (from R49) through CR41 and through Q16's collector.

An equilibrium point is reached where Q16's base current is just enough to hold Q16 on the verge of saturation. CR37 and CR38 reverse bias Q16's base-emitter junction when Q16 shuts off. At that instant T3's secondary voltage is about -6 V, and this pulls the base of Q16 to about -4 V with respect to the emitter. CR42 prevents current from flowing through Q15's base-collector junction during this turn off time.

2.2.4.3 Regulator

The regulator serves two purposes:
First, it prevents the 116 Vdc supply from exceeding about 130 Vdc, and;
Second, it detects power supply fault conditions.

As a voltage regulator, part of Z2, along with Q2 and Q3, is used to form an amplifier which shuts off the switching regulator when the 116 V supply increases beyond 130 Vdc. R9, 10 and 11 form a voltage divider that reduces the 116 V to about 8.5 V and drives a transistor with a zener (reverse biased base-emitter junction) in series with the emitter.

If the voltage increases, the transistor turns on, and this turns Q2 on. Q2 is current limited to 1 ma. by R15, and Q2's collector current flows into Q3°s emitter then down through R16 to Q13 which shuts off the switching regulator. (R16 protects the high voltage transistor, Q3, from possible fault conditions.) R14 provides a voltage drop which feeds back through R13 to give positive feedback (hysteresis) to the regulator. In normal operation, the 116 Vdc supply is controlled by Z1 and its associated circuitry.

This results in a control signal to Q13 that lets the switching regulator put out bursts of power by turning on for 5 to 20 power cycles then shutting off for a while. CR2 and CR5 limit the voltages that run the regulator.

The fault detection circuitry of the controller/regulator is quite complex and can best be understood by considering a power turn on situation.

When the 235 is switched on, the switching regulator immediately goes into a free-run oscillatory mode which results in a current of about .5 A into C7. This charges at about 5 V/msec. R20 and C3 hold the regulator off during this initial start-up phase.

At voltages below about 100 V, RN1(pins 7-8) holds pin 5 of Z3 low which causes the DISABLE line to go high. This keeps the outputs of Z4 high and thus the drive to the inverter circuit is kept low. When C7's voltage finally reaches 100 to 105 V, CR8 and RN1 (pins 5-6) overpower RN1 (pins 7-8) and pull pin 5 of Z3 high which causes the disable line to go low.

The oscillator now drives Z4, which drives gates that drive the inverter circuitry. Thus, the inverter does not turn on until the 116 V supply is close to full voltage.

While C7 is charging, so is C2 which turns on Z2 at pin 12. This pulls Z2 pin 6 low and prevents the high DISABLE signal from turning on Q3, thereby shutting down the switching regulator.

When the 116 V is finally attained, Z1, which monitors the 5 Vdc line, assumes control of the switching regulator through R14 and Q3.

If an overload or short circuit condition exists, the inverter draws more than .5 A of current and discharges C7 in spite of the switching regulator's efforts to keep it charged.

When the inverter supply voltage drops to about 90 V, RN1 (pins 7-8) pulls pin 5 of Z3 low which sends the DISABLE line high. This freezes Z4, thereby shutting down the inverter; and also turns on Z2 pin 6 through R19. This transistor overrides Q2 and turns Q3 on, which in turn shuts off the switching regulator.

With the inverter off, the supply voltage for the regulator/controller (normally 6 V) drops; and this, through CR3 and CR4 pulls pin 3 of Z2 low causing that transistor to turn on and therefore Q2 to turn on. The switching regulator is then held off.

To power the supply back up: turn off power; wait 15 seconds for all the capacitors to discharge; then turn the power back on.

In the event of a power line failure the power supply can run the 235 for a few missing line cycles because of the stored energy in C26 and C27. When their total voltage drops to about 200 V, Q4 is turned on by R45, CR35 and R25 (CR36 normally keeps CR35 back-biased). OC2 turns on which signals the microprocessor that power will soon fail. The DISABLE line is pulled low through CR10 to keep the switching regulator and inverter running for the duration of the loss of power.

2.2.4.4 Oscillator, Driver, and Inverter

The oscillator circuit is a CMOS R-C oscillator that normally free runs at about 26khz. This gets divided in half by Z4 which drives the CMOS inverters that drive Q5, 6, 7 and 8. They, in turn, drive the power transistors, Q10 and Q11.

The oscillator can be synchronized at a higher frequency than its free run frequency by driving Z2 pin 9 from pulse transformer T2. In normal operation this driving frequency is 30.72khz. This results in a 15.36khz drive signal to the inverter.

Z4 drives the Z3 inverters through R-C networks which add about lusec delay to turn on, but zero delay to turn off of the power transistors. Thus, for example, when Q10 is turned off, there is about a micro-second of delay before Q11 turns on. This prevents Q10 and Q11 from being on simultaneously.

Diodes CR13 through CR16 form Baker-clamp drive circuits that prevent Q10 and Q11 from saturating when conducting. C10 and C11 are speed up capacitors that result in fast turn-on and turn -off switching. CR18 through CR21 rectify a secondary winding of T1 and provide the 6 V supply used by the control circuitry.

2.2.4.5 Output Rectifiers, Filters, and Regulators

CR22 thru CR25 and CR27 thru CR30 rectify two secondary windings of T1 to give +5, +16, and -16 Vdc. These output lines have LC filters to minimize ripple.

The logic 5 V supply also has over voltage protection (Q12) which shorts the supply if the voltage rises much above 6 V. This overloads the inverter and results in a systematic shut down of the power supply.

The output lines phase1 and phase 2 are used to drive the FEM's and any option card with an isolated power supply. Since these lines are phase locked to the master oscillator, they can be used for precise timing as well as power applications.

The LOGIC +5V output is filtered by L2 and C17 to form a 5 Vdc supply for the display LEDs. auxiliary +12 and -12 Vdc supplies are obtained from the unregulated +16 and -16 Vdc supplies, respectively, by regulators Z5 and Z6.

The LOGIC +5V output is regulated by Z1, which compares the 5 volt output with a reference voltage from CR1. Z1 drives an opto-isolator, OC1, that controls the regulator, which, in turn, controls the 116 volt line through the switching regulator. Only during start-up or a fault condition does the regulator take control.

2.3 Front End Module (FEM), General

There are five FEM types. These following paragraphs describe all five types, which have many circuits and functions in common. The FEM types are:

Name	PCB Assy	Mechanical Assy
Solid-state FEM	230-4400	231-5001
Reed Relay FEM	230-4410	231-5002
Current Xmtr FEM	230-4411	231-5002
High Voltage FEM	230-4412	231-5004
RTD FEM	230-4430	231-5010

The FEM is a 20-point multiplexer that drives an analog to pulsewidth converter. Digital communication to the FEM is serial, using a 16-bit data stream. The FEM's have 22 addressable channels, with programmable gain ranges. The Solid-state and Reed Relay FEM's also have a programmable break detect signal. The RTD FEM is programmable for either three or four wire operation.

The first twenty channels are signal input points. The other two channels are a zero channel (for autozero), and a temperature reference diode channel (or autocal for RTD's).

All FEMs share a common analog conversion technique, the Solid-state and relay multiplexers are similar, but warrant separate descriptions. The digital communications circuits are common among all FEMs. The digital communications description also includes some repetition of description from the PIA circuit theory (refer to 2.2.2), since the interface is best understood as an entity.

2.3.1 Analog Conversion Circuits

All FEM types share a common analog conversion technique. Figure 2-2 is a block diagram of the analog portion of a FEM. An input signal is first selected by a multiplexer whose output is selected from a bank of multiplexers by a submultiplexer. This selected signal is filtered, amplified, and then digitized.

The analog to digital converter (A/D) is a dual slope integrating type, with an integrator amplifier whose output drives a zero crossing amplifier. The time at which the zero-crossing is detected (output from the zero- crossing amplifier) is directly proportional to the analog input voltage.

The input filter is a conventional unity-gain buffer with positive feedback. However, it is utilized in an unconventional manner; the output being taken from the input to the buffer, rather than from the output, to avoid voltage drift in the buffer.

The pre-amp normalizes all plus full scale input voltages to +2.2v, and contains noise reduction circuitry that results in converted values stable to within +/- 0.5 microvolt.

The pre-amp output is fed to an integrator with auto-zero circuitry, for low voltage drift, which also stores a negative full scale voltage. Storage of the negative full scale voltage is equivalent to adding a constant voltage to the pre-amp output. This allows a single polarity reference voltage to be used. The single polarity reference eliminates zero gap problems encountered in dual polarity reference voltage techniques.

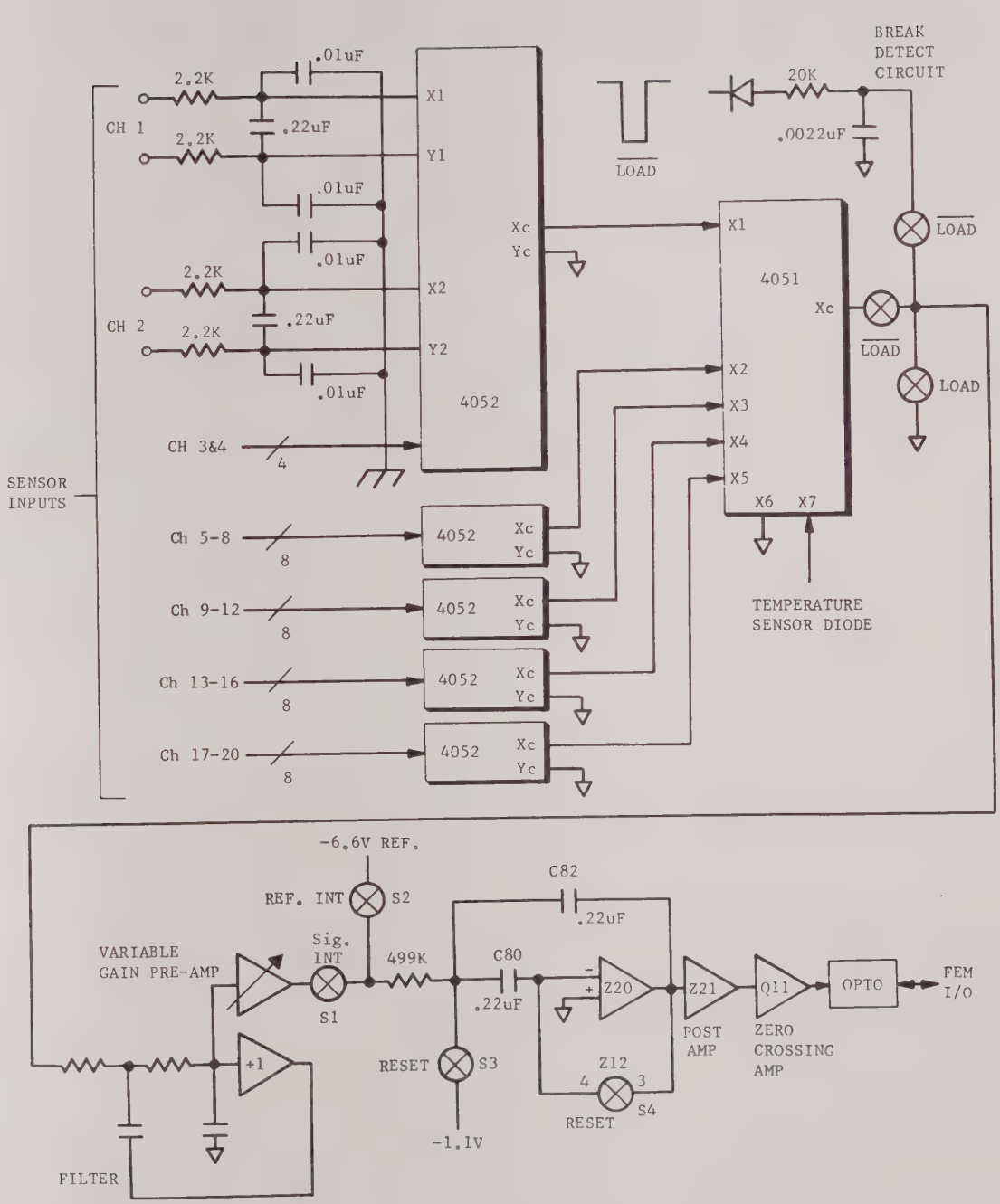

FIGURE 2-2. BLOCK DIAGRAM, SOLID-STATE FEM

NOTE

Since the RTD FEM is unipolar, the negative full scale voltage is set at zero volts.

Offset and negative full scale voltage storage is accomplished as described in the following subparagraphs: follows:

a) During reset, while the input filter and pre-amp are settling to the input voltage, switches S1 and S2 are open; S3 and S4 are closed.

b) Due to feedback action, the input of the integrator is driven to the integrator offset voltage.

c) Since both the input and the output of the integrator are at the integrator offset voltage, both C80 and C82 are charged to -1.1v plus the integrator offset voltage (zero volts instead of -1.1 for the RTD FEM).

d) When reset terminates and signal integrate starts, S3 and S4 open, S1 closes, and S2 remains open.

e) The pre-amp will try to drive the summing junction positive through the 500k ohm resistor. The integrator input terminal now sees a voltage equal to its offset voltage plus a small error voltage. By definition the integrator interprets the offset voltage as zero and responds only to the error voltage. The integrator will drive the summing junction (the junction of the two capacitors) to -1.1v, since C80 and C82 are both charged to -1.1v (zero volts for the RTD FEM).

f) The integrator output will move negative in a ramp-like fashion (see Figure 2-3), feeding back a correction voltage to maintain the summing junction at -1.1v. As a result, a current flows through the 500k ohm resistor proportional to the pre-amp output plus 1.1v. This current charges C82. Because the integrator is an FET input amplifier with very high input resistance, C80 will not discharge.

g) The integrate cycle ends (100ms); S1 opens and S2 closes.

h) The -6.6v reference will try to drive the summing junction negative through the 500k ohm resistor. The integrator output will now ramp positive. C4 will be charged by a current through the 500k ohm resistor determined by -6.6v plus 1.1v.

i) The integrator output will go from a negative voltage, caused by the input, toward zero, driven by the reference. When the voltage reaches zero, the post-amp and zero-crossing amplifier will transmit a pulse to the mainframe.

Figure 2-3 illustrates the integrator output and gives the pertinent equations for the signal integrate and reference integrate cycles. Solving the two expressions for -v gives:

$$-v = T1(Ex+1.1)/RC4 \quad \text{and} \quad -v = T2(6.6-1.1)/RC4$$

equating: $T1(Ex+1.1)/RC4 = T2\ 5.5/RC4$

produces $T2 = T1(Ex+1.1)/5.5$ for all FEMs except
$T2 = T1(Ex)/6.6$ for the RTD FEM

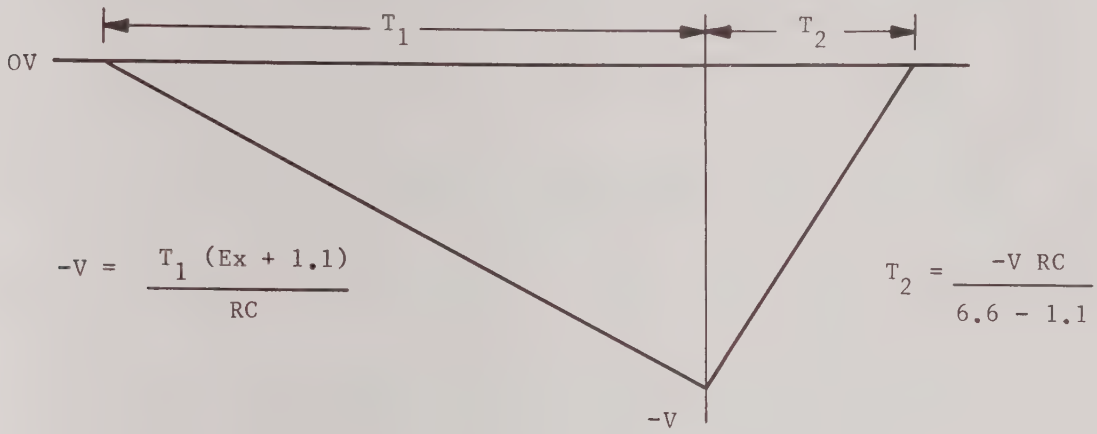

FIGURE 2-3. INTEGRATOR OUTPUT

This equation for the input transfer function is converted by software into a signed decimal number, and assigned engineering units. The software periodically takes a reading with Ex forced to zero and stores this value. When each input reading is taken the stored value is subtracted.

2.3.2 Solid-state Multiplexer

The Solid-state Multiplexer (mux) utilizes CMOS switches (Z1-Z5) for selecting the desired input channel. Figure 2-1 shows the input filtering for two channels (in the actual circuit all channels have input filters). These input filters are necessary to reduce RFI currents, which, if not filtered out, would be partially rectified by the analog input circuitry and show up as microvolt level signals (0 to 100 microvolts). The .01 uf capacitors return RFI currents to the chassis and minimize their effect.

The CMOS switches used are 4052 dual 4-channel multiplexers selected for their low leakage and low offset voltage. Both high and low leads are switched for differential channel selection. The 4052 outputs are sub-multiplexed by Z7 (a 1-of-8 mux chip). Sub-multiplexing reduces, by five, leakage current effects, for increased accuracy when measuring microvolt level signals.

The sub-multiplexer also selects zero volts as an input, or the temperature sensor diode for thermocouple compensation. The zero volt input is utilized, as previously mentioned, for software conversion of the offset transfer function to a bi-polar transfer function.

The selected input voltage is gated by additional switches (Z6) to minimize the effects of channel address changing (during this time the input is grounded), and to introduce a break detect signal.

Break detect is accomplished by charging capacitor C64 during channel selection via Q14, and then discharging C64 through the selected channel source resistance. In the event of a break, the channel will not discharge the capacitor, and a reading of negative overload will result.

2.3.3 Reed Relay Multiplexer

The relay mux circuitry (see Figure 2-4) is nearly identical to the solid-state mux. The obvious exception is the fact that relays are used for channel selection instead of CMOS switches. Additional differences are in the configuration of the RFI filters and the absence of a sub-multiplexer chip.

The RFI filter for the relay mux is configured differently for two reasons: First, the relay contacts will not rectify, so a common differential capacitor can be used; second, large common mode voltages are anticipated in the relay mux, so smaller per channel capacitors are necessary to keep common mode currents to earth within limits.

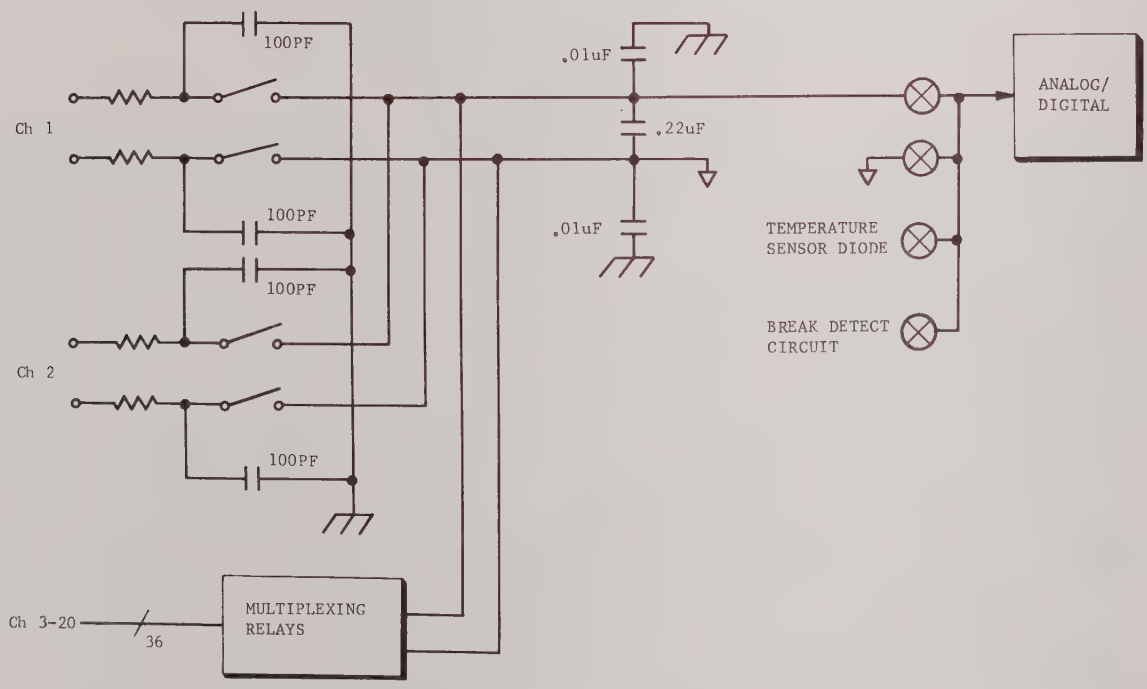

FIGURE 2-4. BLOCK DIAGRAM, REED RELAY MULTIPLEXER

2.3.4 RTD Multiplexer

The RTD mux is very similar to the Solid-state mux; the voltage leads being scanned identically. However, a floating current source has been added, the minus full scale voltage is no longer stored on the integrator capacitor, and the A/D reference is derived from the floating current source.

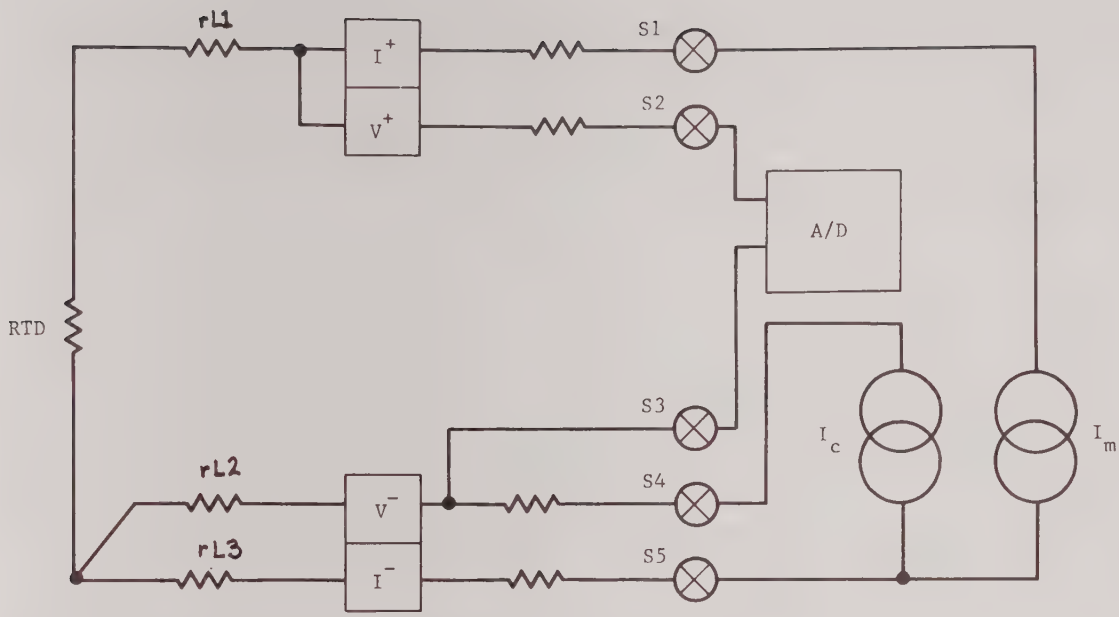

FIGURE 2-5. THREE-WIRE RTD CONFIGURATION, ONE CHANNEL

Figure 2-5 shows one channel of the RTD mux and illustrates the measurement principles involved. A floating current generator (derived from an independent transformer winding on the power transformer) drives a current Im through S1 and S5 to create a voltage drop across the RTD. Switches S2 and S3 connect the RTD, as a voltage source, to the A/D converter. The A/D input voltage is proportional to the RTD resistance.

The additional current generator, Ic, and the switch S4 are included to compensate voltage drops in the RTD interconnect leads. With Ic "off", the voltage sensed by S2 and S3 includes a drop Imrl. There is no contribution due to rL2 or rL3 since no current flows in rL2, which is connected to the high input impedance A/D, and S3 senses the voltage before the drop in rL3.

With Ic "on", an additional term -Icrl2 is added to the voltage sensed by S2 and S3. Since the lead resistance rL1, and rL2 are nearly equal; making Ic equal to Im eliminates lead resistance errors. However, if rL1 and rL2 errors must be completely eliminated, this can be done by adding a fourth wire from the top of the RTD to V+. In addition, the jumper from V+ to I+ must be removed, and Ic turned off. Under these conditions S2 and S3 will sense the voltage across the RTD without any contribution due to rL1 and rL2.

Figure 2-6 shows the current generator switching utilized in the RTD mux. During reset and signal integrate, the current Im is switched through the selected RTD. During reference integrate all switches are off except SR1, SR2, and SR3. The current Im flows through Rref and forms a Thevenin equivalent of a battery with an output voltage ImRref and a source resistance Rref. The positive terminal of this voltage is grounded by SR2; this voltage then becomes a negative reference.

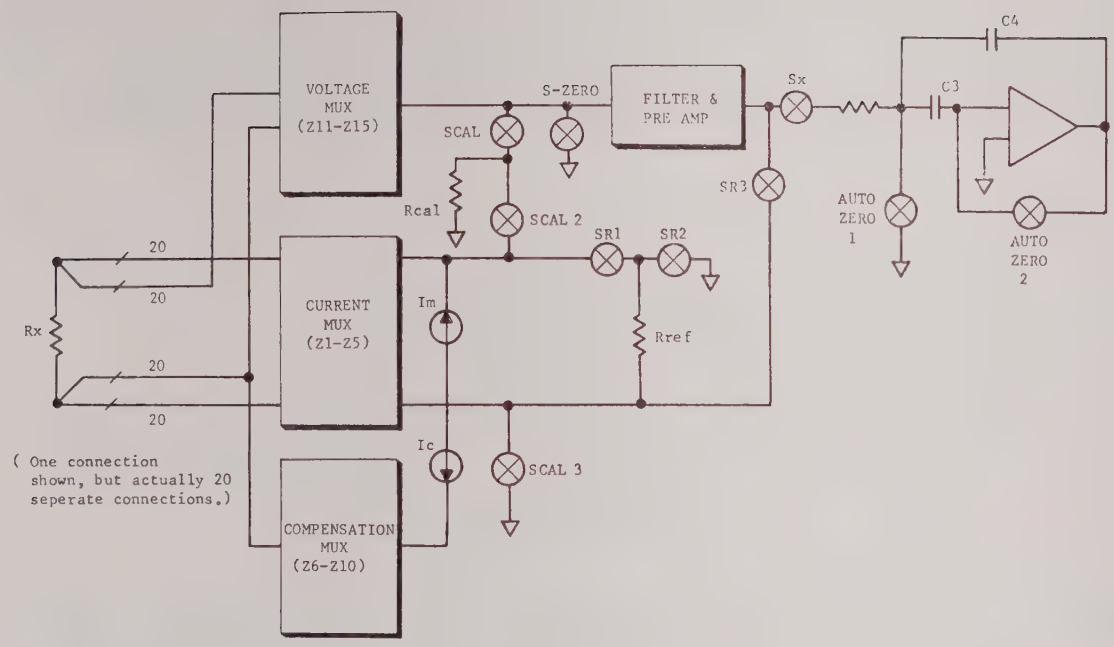

FIGURE 2-6. RTD MULTIPLEXER CURRENT GENERATOR SWITCHING

Since the same current excites the RTD and produces the reference voltage, it does not have to be a precision current. The current appears in both numerator and denominator of the transfer function and cancels. To further increase the accuracy of measurement, calibration resistor Rcal is included.

During reset and signal integrate, the current Im is switched through Rcal if the RTD mux is addressing the autocal channel. The calibrate resistor is thus measured and the resultant reading stored for scale factor correction.

Similarly, the switch S-zero grounds the input for a zero reading, and a correction factor for zero is stored. With these two measurements the RTD mux can automatically calibrate itself.

Since the RTD measurement voltage is unipolar, it is not necessary to add a constant to the input voltage. The switch S-autozero is connected to ground, and the only voltage stored on the capacitors is the integrator offset voltage, which is thereby autozeroed out.

2.3.5 Digital Communication

The communication link to the analog module is two twisted pairs in a foil shield. One pair is driven by a 15khz square wave that provides power to the analog module and a clock for timing in the analog module. The other pair is a bi-directional link which transmits a convert start pulse string to the analog module and receives a convert complete pulse from the analog module.

The convert start pulse is the first of 16 pulses that transmit instructions to the analog module in a serial mode. Contained in this serial pulse string is: channel address, break detect enable or 4 wire enable, and gain selection.

Figure 2-7 is a block diagram of the data receiver scheme of the analog module. The D input of the shift register is driven from a 15 kHz square wave which represents alternate "ones" and "zeroes". The shift register is clocked by the data, shifting "ones" or "zeroes" depending on the state of the 15 kHz clock as the data clocks the shift register. Since the shift register is 8 bits long, only the last 8 bits transmitted are retained in the register.

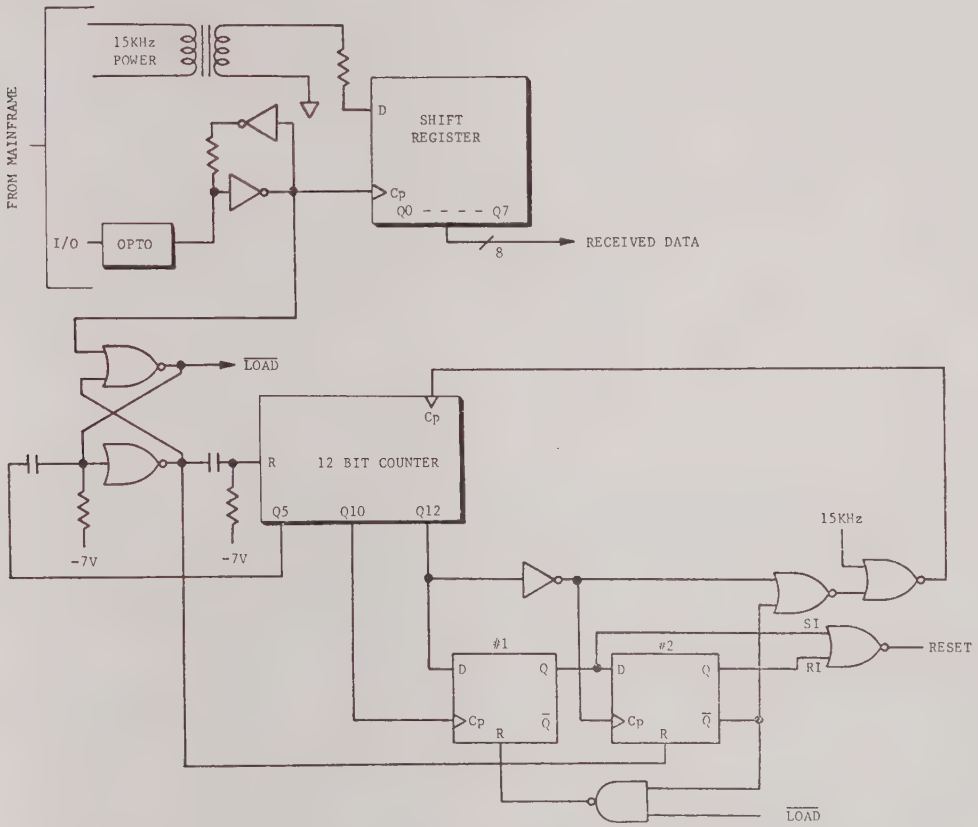

FIGURE 2-7. BLOCK DIAGRAM, DATA RECEIVE/DECODE CIRCUITS

When the first pulse is transmitted a counter on the PIA card is started. Similarly, when the first pulse is received by the analog module, a counter is started in the FEM. Both counters are counting the same 15 kHz square waves so synchronization is established.

The eight bits retained will be decoded as shown:

G1	G2	BD	C	B	A	B'	A'
last bit							first bit

Channel address bit weights are: A'=1 B'=2 A=4 B=8 C=16
When Break Detect bit BD is set low (0), an open circuit at the input will cause a negative overload.

Voltage/Thermocouple FEM

When Gain bit G1 =	0	0	1	1
and, Gain bit G2 =	0	1	0	1
then Gain Range =	20mv	80mv	400mv	2volt

RTD FEM

When Gain bit G1 =	0	0	1	1
and, Gain bit G2 =	0	1	0	1
then resistance =	230ohms	390ohms	650ohms	not used

The channel number is given by the binary number +1 formed by CBAB'A'.
Channels 21-24 are ZERO
Channels 25-28 are:
Volt/TC FEM: Temp Reference Diode
RTD FEM: 225ohm autocal resistor

The FEM data must be re-mapped for proper transmission. The data is transmitted PA7 first and PA0 last. However, the received data is interpreted with the first received bit as the LSB. The consequence of this is that the transmitted data must be loaded as shown:

PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
A'	B'	A	B	C	BD	G2	G1

The data to be output is sent through a PIA A register (femporta) located at 2204h and controlled (femctrla) through location 2205h. The data to be output must be loaded in two bytes. These two bytes are loaded into shift registers selected by the PIA B register (femportb) located at 2206h and controlled (femctrlb) through location 2207h.

The shift registers are loaded by CB2 ANDed with either PB7 or PB6. FEM data is loaded at CB2 AND PB7; CB2 AND PB6 is normally loaded with -1, to satisfy the requirement of a ONE for the first bit transmitted. Communication is initiated by the 15 Hz clock from the PIA.

Figure 2-8 is a block diagram of the bit stream encoding circuit. The negative transition of 15 Hz sets a flip-flop which opens a pulse gate, and causes the contents of a 16-bit shift register to be serially transmitted at a 15 kHz rate. Data is output in an encoded form with positive output transitions from the shift register determining "1"s and "0"s in conjunction with the logic state of the 15 kHz clock at the moment of transition.

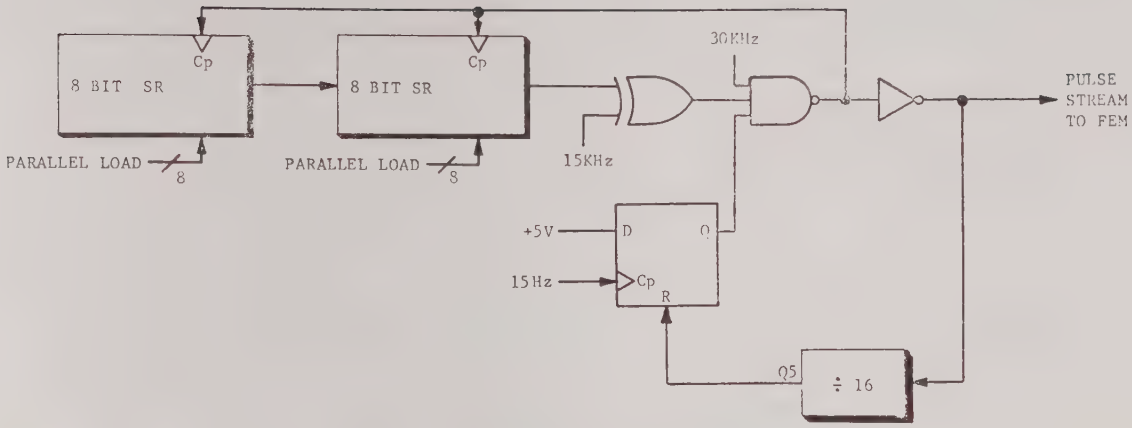

FIGURE 2-8. BLOCK DIAGRAM, DATA SHIFT/ENCODE CIRCUITS (PIA)

The data is encoded by an Exclusive-OR gate, and the 30 kHz clock, which forces positive transitions to occur at the center of the 15 kHz high or low state. The Exclusive-OR gate compares the shift register output to the 15 kHz clock and inhibits negative transitions when they are the same. Since the output is held high there is no positive edge, with the net result that positive transitions occur only during the 15 kHz state opposite from the data. Decoding is done by using the positive edge to strobe the opposite phase of 15 kHz into a shift register.

Figure 2-9 shows pertinent waveforms for encoding serial transmission of Channel 1 in the function 5 (one volt range) mode. Notice that the first 8 bits transmitted are "1"s followed by the data. The receiver only retains the last 8 bits transmitted, so these bits serve only to notify that data transmission is starting.

The encoded bit stream is counted by a binary counter. When 16 bits have been transmitted, the Q5 output of the counter resets the flip-flop, which in turn shuts off a pulse gate, and the system waits for the return of the zero crossing.

The bit stream is generated on the PIA board, and is directed to a 74LS156 1-of-8 multiplexer that drives the output line directly.

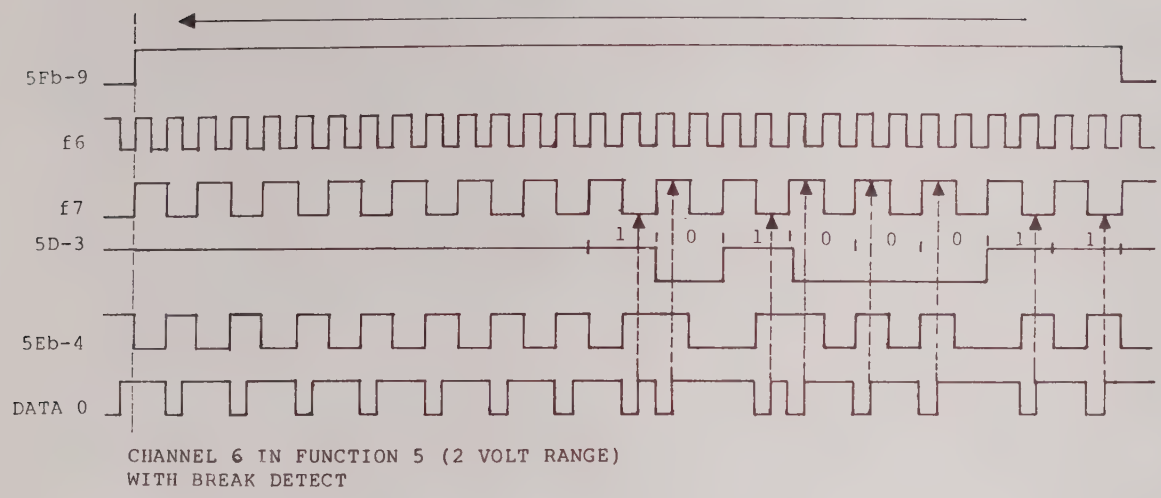

FIGURE 2-9. TIMING DIAGRAM, DATA ENCODING FOR SERIAL TRANSMISSION

Figure 2-10 illustrates one channel of the transmitter-receiver pair. The TTL output drives the FEM input line directly, and the pulse is coupled to the FEM through a 220 ohm resistor on the FEM card which may be selected by connecting to the appropriate input pins on the FEM.

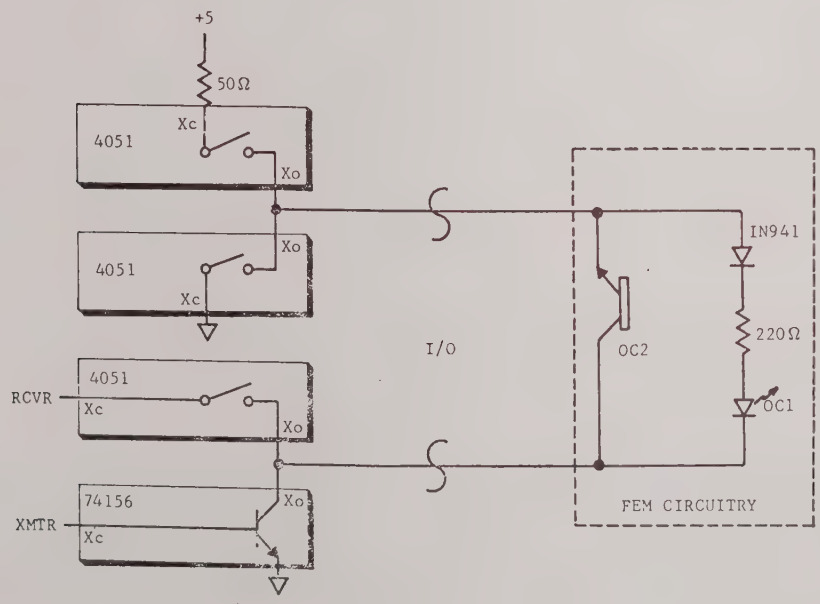

FIGURE 2-10. MAINFRAME TRANSMITTER/RECEIVER PAIR

The zero crossing comes back over the same line used for bit transmission. When the zero crossing occurs, transistor OC2 turns on, which causes an inverter turn off. The PIA reverses the polarity of the lines during data reception utilizing the top multiplexer, which switches that line from +5v to ground. The high state of the inverted received signal is clocked by the 1 MHz system clock into a flip-flop, and strobes the system counter contents into a register.

Since this counter originated the conversion when its content was zero, the present content is a direct measure of the elapsed time from convert start. The dual slope converter generates a time proportional to the analog input, so the counter contains a number directly proportional to the analog input.

2.3.6 FEM Timing

The basic conversion time for each front end module is 333 1/3 ms. This time is divided into intervals of 166 2/3 ms, 100 ms, and 66 2/3 ms as shown in Figure 2-11 below.

During the first nominal 1 ms the channel input is opened and the A/D input is grounded. This is the time that the 16 clock pulses are shifting data through the shift register. After this time the input signal is switched through the multiplexer to the A/D input filter and pre-amp. The input filter and pre-amp are allowed the remaining 166 2/3 ms (less the nominal 1ms) for settling to the input voltage.

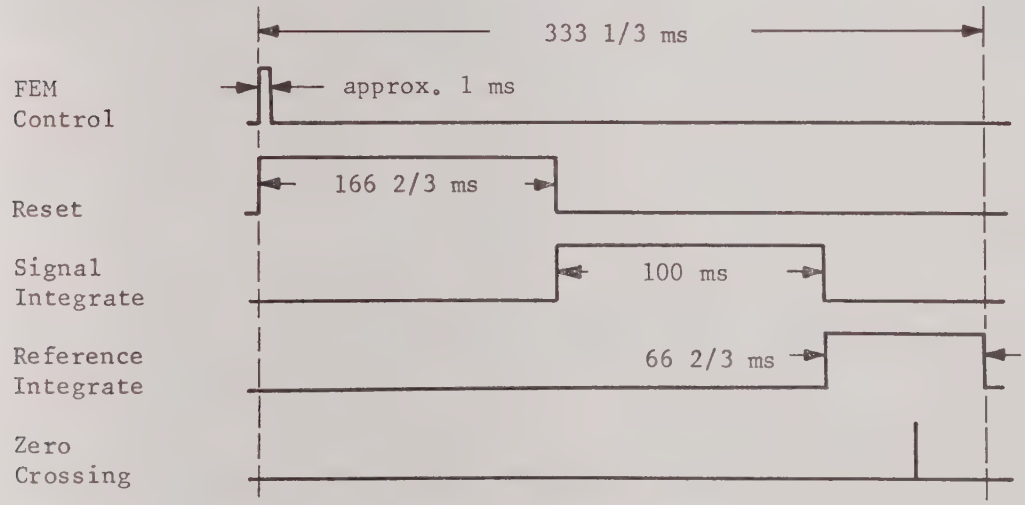

FIGURE 2-11. TIMING DIAGRAM, BASIC CONVERSION CYCLE

The FEM timing waveforms are derived from the logic shown in Figure 2-7. When the bit stream from the mainframe is received, it sets an RS latch formed by two cross-coupled NOR gates.

Setting the latch resets all the logic. The counter is reset by the transition through an RC network and, the two D flip-flops are directly reset. The 12 bit counter counts 15 kHz derived from the mainframe. After 16 counts, the Q5 output goes high, and the RS latch is reset.

The counter continues to count; when Q12 goes high and Q10 makes a positive transition, D flip-flop #1 is set. This occurs after 2560 counts, or 166 2/3 ms (the clock is slightly faster than 15 kHz). Setting flip-flop #1 causes signal integrate (SI) to go TRUE, and RESET to go false (since RESET is the NOR of SI and RI).

When Q12 then goes low, flip-flop #2 is set, which resets flip flop #1 through a NAND gate. This causes reference integrate (RI) to go high, and SI to be terminated. This occurs after 4096 counts, or 266 2/3 ms.

Signal Integrate time is thus 100 ms (266 2/3 ms - 166 2/3 ms). If the counter continued to count until Q12 went low, the NOR gate monitoring RI(not) and Q12(not) would shut off the 15 kHz clock gate and stop counting--waiting for the next bit stream. This would occur after 6144 counts or 400 ms. However, the mainframe normally sends bit streams every 333 1/3 ms, so this state is not reached.

The mainframe can drive up to five FEMs. The conversion timing of these FEM's is interlaced so that each one starts a conversion every 66 2/3 ms.

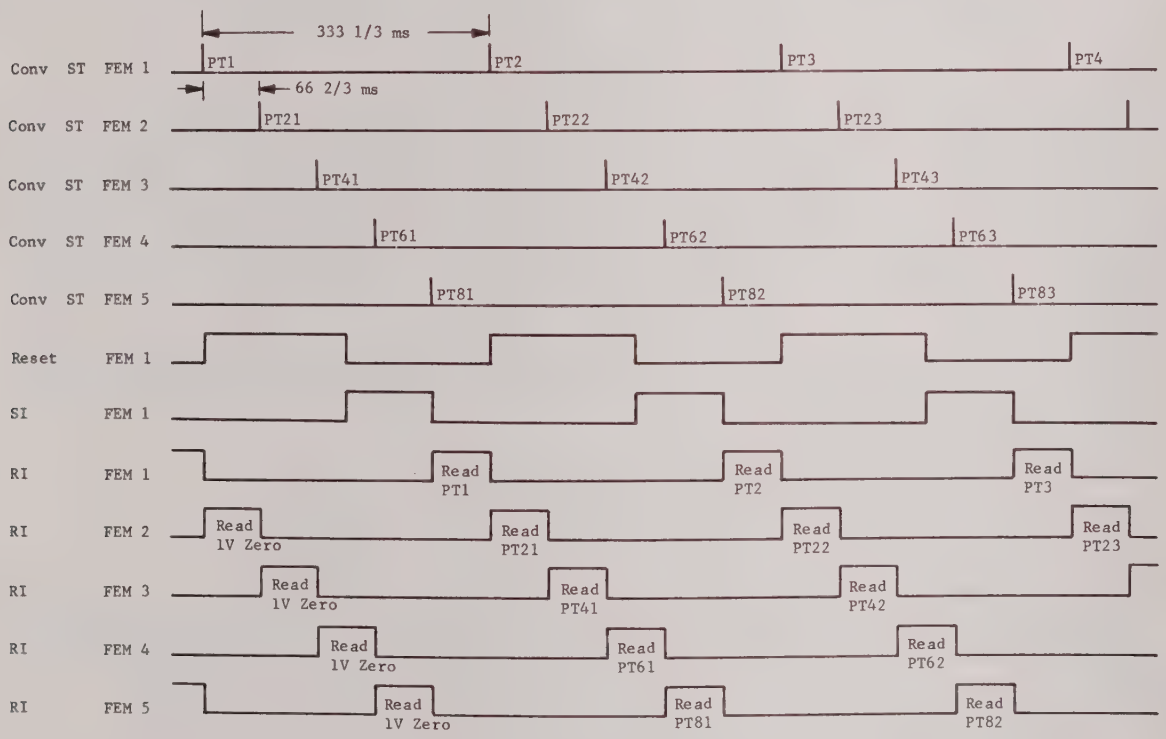

FIGURE 2-12. TIMING DIAGRAM, POINT SCANNING SEQUENCE

Referring to Figure 2-12, the mainframe sends a convert start pulse to points 1, 21, 41, 61, and 81 in sequence (each pulse 66 2/3 ms apart). This sequence takes 266 1/3 ms; and at its conclusion the CPU returns to point 1 and looks in a 66 2/3 ms window to read the converted data, then starts a conversion on point 2.

In sequence, 66 2/3 ms apart, the CPU then takes data and starts new conversions on points 21 and 22, 41 and 42, 61 and 62, 81 and 82 respectively. This scanning sequence continues with each module point address advancing by one until all 100 points have been scanned.

This sequence is followed whether or not any given module is plugged in. It should be noted that removing modules does not provide any additional time for the remaining modules, since all modules are converting simultaneously.

After 100 points have been scanned, the CPU then scans two of the added module functions (zero,temp,cal). Another 100 points are scanned and another two added functions are scanned and so on. Consequently, any given point is scanned every 7.333 seconds (22 times 333 1/3 ms.) The added functions are: four zero readings (one for each gain range) and two temp readings. Or, for RTD's, three zero readings and three cal readings. These functions are scanned once every 29.333 seconds (7.333 seconds times four readings). The scanning sequence with the functions is:

2 volt zero,	20 mv zero,	20 points
2 volt zero,	80 mv zero,	20 points
2 volt zero,	400 mv zero,	20 points
Ref junction,	2 volt zero,	20 points

This sequence ensures that all low level readings will be preceeded with a zero reading on the two volt range. This is necessary to fully discharge the input filter before low level readings are read following a high level reading.

This does not avoid point to point dc crosstalk, but it does avoid crosstalk between the temperature diode reading and point one, or point 20 and the 20 mv zero reading. There is no crosstalk problem between RTD points and RTD calibration readings. But, the RTD follows a similar sequence so the same scanning program can be used.

The scanning sequence can be modified by programming a point in the CAL mode. In this mode, only the point under CAL and the added functions are scanned. The scanning sequence will be:

2 volt zero,	20 mv zero,	2 volt zero,	point,
2 volt zero,	80 mv zero,	2 volt zero,	point,
2 volt zero,	400 mv zero,	2 volt zero,	point,
2 volt zero,	Ref Junction,	2 volt zero,	point.

The CAL point will be converted every 1 1/3 seconds (4 times 333 1/3); and the added functions are converted every 5 1/3 seconds while a point is under CAL.

2.3.7 System Algorithm

The mainframe display is derived by digitizing the zero point and storing that value (ZERO). Subsequent conversions subtract ZERO from the A/D counts. The ZERO reading for any range must be read with the corresponding gain bits set for that range. The algorithm for all FEM's except an RTD FEM is:

$$R = Rn - ZERO$$

Where:
R is the compensated output counts
Rn is the counts measured on point n
ZERO is the counts measured with zero input
ZERO = 20879 +/- 400 counts (same gain as Rn)

For an RTD FEM the counts must be multiplied by an autocal constant in addition to subtracting ZERO. The algorithm for the RTD FEM output is:

$$R = (Rn - ZERO)(CORRECT)/(CAL - ZERO)$$

Where:
R is the compensated output counts
Rn is the counts measured on point n
ZERO is the counts measured with zero input
ZERO = 300 +/- 50 counts (same gain as Rn)
CORRECT is the correct counts for 225 ohms
CAL is the counts measured for 225 ohms

230 ohm range	CORRECT = 64,110
390 ohm range	CORRECT = 37,809
650 ohm range	CORRECT = 22,500

2.4 OPTION BOARD ASSEMBLIES, GENERAL

The following printed circuit board assemblies comprise the option boards:

1. Memory Extension (Math Functions) Board
2. Alarm Monitoring Board
3. Alarm Relay Board
4. Serial I/O Port #2
5. Digital Inputs Board

The option boards extend the capability of the Digitrend 235; providing additional functions depending on the user's requirements.

The Memory Extension board has provisions for up to 5K-bytes of additional RAM (random access memory) and up to 32K-bytes of additional ROM (read only memory) or EPROM (eraseable programmable read only memory). This board carries the program used to provide math functions, and can be used to carry additional programs for other functions. This board also features an Auto Restore Clock which keeps track of time in the event of a power failure. When instrument power is restored, the clock is automatically restored to the current time.

The Alarm Monitoring board provides alarm capability to data points; producing an alarm log and/or relay actuation when an alarm condition is detected. The Alarm Monitoring board interfaces with the Alarm Relay Panel (2 ea. max) to provide relay actuation.

The Alarm Relay Panel contains 16 relays and their associated driver circuitry. It also contains an encoder circuit which can encode up to 20 switch inputs. The Alarm Relay Panel is interfaced with an Alarm Monitoring card to provide relay actuation when an alarm condition is detected.

The Serial I/O Port #2 board provides a second serial data input/output port which is both RS-232 and 20 mA current loop compatible.

The Digital Inputs board provides inputs for either digital data or status data. It also provides up to 48 event sense inputs.

2.4.1 Memory Extension Board Assembly, General

Assembly: 231-4462-00
Schematic: 231-6462-00

The Memory Extension board allows for 5K of RAM, and 32K of 2716 type EPROM (or pin compatible ROM), to be mapped into any location in the system memory map, in 256 (or in some cases 128) byte blocks of contiguous or noncontiguous memory. This board supports software for Math Functions (Option M) and Digital Inputs (Option D) in addition to the software/hardware for the Auto Restore Clock.

The Memory Extension board is provided with battery back-up for its RAM memories and Auto Restore Clock, to preserve data stored in RAM and to ensure continuity of the software clock in the event of a power failure.

The Memory Extension board can be divided into seven functional sections:

1. RAM
2. ROM
3. DECODING CIRCUITS

4. TIMING CIRCUITS
5. BUS BUFFERS
6. BATTERY BACK-UP CIRCUIT
7. AUTO RESTORE CLOCK

2.4.1.1 RAM

The RAM memory section has provisions for up to ten 1K x 4 CMOS RAM devices arranged as a 5K x 8 memory array.

The RAMs are paired, with one RAM device of each pair used to store the upper four bits of the data word, and the other RAM device used to store the lower four bits of the data word.

For example, ICs 1E and 2E are paired together, with 1E used to store the upper four bits, and 2E used to store the lower four bits. The RAM pairs are 1E and 2E through 1M and 2M. The board can be populated in 1K increments up to a total of 5K.

The RAM data bus is divided into two parts: the UPPER RAM DATA BUS, and the LOWER RAM DATA BUS.

The UPPER RAM DATA BUS is connected to ICs 1J, 2J, 1K, 2K, 1L, 2L, 1M, and 2M.

The LOWER RAM DATA BUS is connected to ICs 1E, 2E, 1F, 2F, 1G, 2G, 1H, and 2H.

Both RAM data buses are buffered from the BOARD DATA BUS by bi-directional, tri-state data buffers 1A and 2A. The UPPER RAM DATA BUS is buffered by 1A, while the LOWER RAM DATA BUS is buffered by 2A.

The direction of data flow through the data buffers is controlled by the BR/(not)W line (refer to DECODING CIRCUITS). When the BR/(not)W line is logic "high", and the buffer is enabled, the flow of data is from the RAM DATA BUSes to the BOARD DATA BUS. When the BR/(not)W line is logic "low" the flow of data, when the buffer is enabled, is from the BOARD DATA BUS to the RAM DATA BUSes.

The BR/(not)W line also controls the operation of the RAM devices. When the BR/(not)W line is logic "high", the selected RAM is in a "read" mode. When the BR/(not)W line is logic "low", the selected RAM is in a "write" mode. The RAM pairs are selected by way of the RAM select lines, (not)0 through (not)7, that are generated by the DECODING circuitry.

The upper RAM data buffer, 1A, is enabled by a logic "low" on the (not)URDE line which is generated by the decoding circuitry (refer to DECODING CIRCUITS). The lower RAM data buffer, 2A, is enabled by a logic "low" on the (not)LRDE line which is generated by the decoding logic.

2.4.1.2 ROM

The ROM memory section consists of sixteen 2716 type EPROMs (or pin compatible ROMs) arranged as a 32K x 8 memory array. These EPROMs are 2K x 8, and are paired to form eight 4K x 8 blocks. The EPROM/ROM pairs are 4E and 5E through 4M and 5M. 2732 type EPROMs (or pin compatible ROMs) may be used with each device, replacing two 2716 type devices. The 2732 type EPROMs are 4K x 8, and must occupy the 4(x) position of the EPROM/ROM pair with the 5(x) position left empty. The maximum array size is still 32K x 8.

The ROM DATA BUS is buffered from the BOARD DATA BUS by a tri-state data buffer, IC 3A. The ROM DATA BUS buffer is enabled by a logic "low" on the (not)ROBE line, that is generated by the DECODING circuitry.

The EPROM/ROMs are selected by a logic "low" on one of the enable lines, (not)E0 through (not)E7, generated by the DECODING circuitry.

2.4.1.3 Decoding Circuits

The decoding section of the Memory Extension board is centered around two concepts of operation. First, the memory address from the CPU is decoded by a 512 x 8 fused link PROM, IC 5A, which generates a remapped memory address located on 128 byte boundaries. Second, the memory space is arranged as five 1K x 8 blocks of RAM memories and sixteen 2K x 8 blocks or eight 4K x 8 blocks of EPROM/ROM memories as described in the RAM and ROM paragraphs.

The address remapping PROM 5A is driven by the upper nine system address lines, A7 - A15. This yields the 128 byte remapping boundaries.

The upper three bits of the remapping PROM's output, D5 - D7, are used to drive a 1-of-8 decoder, IC 3C, which is used to select the desired memory block. The PROM outputs, D5 - D7, act as the select inputs to the decoder.

The system (not)VMA signal acts as one logic "low" enable input to the decoder while the system (not)RESET signal inverted by inverter 3Be acts as the second logic "low" enable input.

The REO line acts as the logic "high" enable strobe for the decoder. The REO line is generated by the TIMING circuitry (refer to the TIMING CIRCUITS).

When the (not)VMA signal is logic "low" and the (not)RESET signal is logic "high" in conjunction with a logic "high" on the REO line, the output of the decoder, as selected by PROM outputs D5 - D7, will be enabled, and will go to a logic "low". The outputs of the decoder, 3C, correspond to the enable lines (not)E0 through (not)E7.

The lower four PROM outputs, D0 - D3, are buffered by IC 5C to generate the BA8' - BA11' ROM address lines. The BA11' address line is inverted by inverter 5Da to form the (not)BA11' ROM address line. BA11' and (not)BA11' are used to divide each 4K x 8 EPROM/ROM memory block into a lower (BA11') 2K x 8 memory bank and, an upper ((not)BA11') 2K x 8 memory bank. The lower two PROM outputs, D0 and D1, are again buffered by 5C to generate the BA8'' and BA9'' RAM address lines.

IC 5C is also used to buffer the system clock F1 to form the BF1 clock used by the board, and to buffer the system R/W line to form the BR/(not)W line.

Output D4 of PROM 5A is the (not)ROME, (not)ROM Enable, signal. The (not)ROME signal is programed to a logic "low" state for all remapped EPROM/ROM locations.

An EPROM/ROM is enabled by having its select line, one of the (not)E0 - (not)E7 lines, go to a logic "low" in conjunction with the (not)ROBE line going to a logic "low". The (not)E lines are generated as described above by decoder IC 3C.

The (not)ROBE line is generated by NAND gate 2Bc. NAND gate 2Bc NANDs together the BF1 line, the BR/(not)W line, and the inverted (not)ROME line. The (not)ROME line is inverted by inverter 3Bd. When the (not)ROME line is logic "low", the BR/(not)W line is logic "high", and the BF1 line is logic "high", the output of NAND gate 2Bc, the (not)ROBE line, will be logic "low". The (not)ROBE line is used to enable the ROM DATA BUS buffer (refer to ROM).

The BA10' and BA11' address lines are NANDed together by NAND gate 4Db. The output of 4Db is NANDed with the (not)ROME line by NAND gate 4Dc to form the (not) RAME, (not) RAM Enable, line. The resulting (not)RAME line will be a logic "low" whenever the (not)ROME line is logic "high" (not a ROM address) and either BA10' or BA11' is logic "low".

By using this combination of BA10' and BA11' in the decoding scheme, complete deselection of the Memory Extension board is provided when desired.

The BR/(not)W line is inverted by inverter 5Db and its output is then NANDed with the (not)RWA signal by NAND gate 4Dd to generate the WTC line.

The WTC line will go to a logic "high" whenever the (not)RWA signal is logic "low" or the BR/(not)W line is logic "high". The (not)RWA signal is generated by the TIMING circuitry.

The (not)RAME and WTC lines are used to control the chip select circuitry for the RAM memories. Each of the eight select lines (not)E0 through (not)E7 are connected to one input of a two-input NOR gate. The second input is the (not)RAME line.

The NOR gates used are 1Ca, 1Cb, 1Cc, 1Cd, 2Ca, 2Cb, 2Cc, and 2Cd. The output of each NOR gate is connected to one input of a three input NAND gate. The other two inputs are the WTC line and the BF1 line.

The NAND gates used are 1Db, 1Dc, 2Da, 2Db, 2Dc, 3Da, 3Db, and 3Dc.

The output of one of the NOR gates will go to a logic "high" when one of the select lines, (not)E(x), is logic "low" and the (not)RAME line is logic "low".

The output of the corresponding NAND gate will go to a logic "low" when both the WTC and BF1 lines are logic "high". The output of the NAND gate will sink the emitter of the corresponding transistor, Q2 through Q9, to ground. The base of the transistor is biased by a resistor/capacitor network. The bases of all eight transistors are normally biased ON.

If, however, a system reset should occur, the (not)RESET line connected to the base of Q1 will go to a logic "low" and turn OFF Q1. This will shut OFF the base bias current to transistors Q2 through Q9 thus preventing the RAM from being enabled.

When the NAND gate's output goes to a logic "low", the collector of the corresponding transistor will go to a logic "low" and drive the corresponding RAM select line, (not)0 - (not)7, to a logic "low", thus selecting the RAM.

The RAM DATA BUS buffers are enabled by the (not)URDE and (not)LRDE lines, as described in the RAM paragraphs. These two lines are generated by combining the (not)RAME, UA0, and BF1 signals.

The UA0 signal is the D7 output from the address remapping PROM, 5a. The (not)RAME signal is inverted by inverter 3Bb. The output of 3Bb is connected to one input each of the two three-input NAND gates 2Ba and 2Bb.

The BF1 signal is connected to one input each of the two NAND gates. The UA0 signal is connected directly to the third input of NAND gate 2Ba. The output of 2Ba drives the (not)URDE line.

When the (not)RAME signal is logic "low" and the UA0 and BF1 signals are logic "high", the output of NAND gate 2Ba will be logic "low", causing the (not)URDE line to be logic "low", thus enabling the UPPER RAM DATA BUS buffer 1A.

The UA0 signal is inverted by inverter 3Bf, and the output of 3Bf is connected to the third input of NAND gate 2Bb. The output of 2Bb drives the (not)LRDE line.

When the (not)RAME and UA0 signals are logic "low" and the BF1 signal is logic "high", the output of NAND gate 2Bb will be logic "low", causing the

(not)LRDE line to be logic "low", thus enabling the lower RAM DATA BUS buffer 2A.

2.4.1.4 Timing Circuits

The system clocks, F1 and F1x8 are used to generate the REO line, which is a precessed clock line. The system clock F1x8, is used to clock the timing register IC 4C. The system clock F1, is inverted by inverter 5Dc and acts as the data input to the timing register.

The output of the timing register is the (not)RWA signal, which is coincident with F1 and used by the decoding section to generate the WTC line.

The (not)RWA signal is NANDed with the inverted F1 clock by NAND gate 4Da. The output of NAND gate 4Da is the REO signal, which is used as the logic "high" enable for the 1-of-8 decoder, IC 3C.

2.4.1.5 Bus Buffers

In order to keep the capacitive loading of the system data bus to a minimum, the RAM and EPROM/ROM memory sections have their own individually buffered data buses. In addition, the RAM memory data bus is split into a high order and a low order data bus.

The RAM data buffers are selected in the decoding mode thru the use of the highest bit of the remapping PROM's output, D7. D7 is used to distinguish between the upper and lower address decoding in the master 1-of-8 decoder 3C.

The EPROM/ROM data buffer is arranged to turn on only during an F1 read access to the EPROM/ROM memory space. This prevents an accidental write to EPROM/ROM cycle.

The lower 8 system address lines, A0-A7, are buffered by two separate address buffers. Address buffer 4B drives the ROM ADDRESS BUS, and address buffer 4A drives the RAM ADDRESS BUS. The upper 9 system address lines, A7-A15, are buffered by the address remapping PROM, IC 5A.

2.4.1.6 Battery Back-up Circuit

The RAM memory on the Memory Extension board is provided with battery back-up power. The battery back-up system is similar to the one used on the CPU board except the battery voltage is higher at 3.6 volts in order to accommodate real time clock chip 1L used as an Auto Restore Clock. This scheme automatically removes chip select on a system reset signal, and whenever the RAM memory is being maintained on the battery supply.

On power down, the system tracks Vbb, which follows the main power supply down to the battery voltage level, at which point the battery starts to supply the maintaining power to the RAMs.

Transistors Q10 and Q11, along with battery BT1, and their associated circuitry, make up the battery back-up system.

2.4.1.7 Auto Restore Clock

The Auto Restore Clock (ARC) circuit keeps track of time after a loss of instrument power. When instrument power is restored, the instrument clock is automatically updated by the ARC, and user jobs resume at that point in time.

Operation of the ARC circuit revolves around CMOS real time clock chip, 1L (HI-8000). The ARC resides at address 2000h and 2010h. The frequency of the crystal oscillator used for the ARC is 32.768 kHz.

Decoder 1K selects the operating mode of ARC chip 1L by providing input to the ALE, RD(not), and WR(not) lines. The UPPER RAM DATA BUS is input to AD0-AD7 of the ARC and functions as either an address bus or data bus (AD bus) depending on the state of the ALE input. If ALE is toggled (low-high-low), data on AD bus is received as address/instruction. If ALE is low, data on AD bus is either input or output data.

Power up time information is read from the contents of the ARC°s internal data registers. The coded read instruction of a particular register appears on the AD bus which is latched by the ALE input. A dummy write is then executed by writing zeros to the desired address location (WR[not] low; dummy data being written on AD bus). A read of the desired contents of the previously addressed register is then made when RD(not) is low. The data read from 1L is stored in RAM for later display and log output.

The ARC is initially set by writing the value of the software clock into the ARC counters. The coded write instruction appears on the AD bus which is latched by the ALE input. The data is then written when it appears on the AD bus and WR(not) is low.

2.4.2 Alarm Monitoring Board, General

Assembly: 231-4360-00
Schematic: 231-6360-00

The Alarm board has two basic functions:

1. Control the function of the relays located on the Relay panel.

2. Read the encoded data coming from the key encoder located on the Relay panel.

The Alarm Board is designed to drive two separate Relay panels and to accept encoded data from both Relay panels.

In addition to the control logic for the relay control and data inputs, the Alarm board has provisions for 2K bytes of static CMOS battery backed-up RAM memories to be used to store alarm set points.

The Alarm board can be broken down into six functional sections:

1. BUS BUFFERS
2. DECODING CIRCUITS
3. TIMING CIRCUITS
4. RAM
5. OUTPUT REGISTERS AND OPTO-ISOLATORS
6. INPUT DATA SYSTEM AND CONTROL

2.4.2.1 Bus Buffers

The Alarm board interfaces to the system bus through bus buffers. The address lines A0 through A15, (not)VMA, and F1x8 are buffered by low power schottky TTL inverters.

The control and timing lines F1, R/W, (not)WPRO, and (not)RESET are buffered by an 8T97 driver, IC 5A. The (not)IRQ line is driven onto the system bus by transistor Q6.

The bi-directional data lines, D0 through D7, are buffered from the system data bus, and driven to the system data bus, by a low power schottky TTL, bi-directional bus buffer, IC 1A.

The direction of the data transfer is controlled by the BR/(not)W line, which is inverted by IC 3Bb, and then used to drive the DIR input of data buffer 1A.

When the BR/(not)W line is logic "low", the bi-directional data buffer, 1A, is set to transfer data from the system data bus onto the Alarm board's internal data bus lines, BD0-BD7.

When the BR/(not)W line is logic "high", the bi-directional data buffer, 1A, is set to transfer data from the Alarm board's internal data bus lines to the system data bus.

The bi-directional data buffer, 1A, is a tri-state buffer. It's outputs are enabled whenever the (not)EDB line (refer to DECODING CIRCUITS) is logic "low".

2.4.2.2 Decoding Circuits

The decoding section consists of the following ICs:

3B, 3C, 3D, 4B, 4C, 4D, 4E, 4F, 5D, and 5E

The board select decoding is done by 4B, 5Ec, and 4Af. When (not)BA12, (not)BA14, (not)BA15, BVMA, (not)BRESET, and @M (refer to TIMING) are logic "high", and (not)BA11 and (not)BA13 are logic "low", the board select, (not)BOARD, line will go to a logic "low".

The UA0, Unit Addressed Output, line is decoded by ICs 3Ba, 3Bc, 4Aa, and 4Dc. The UA0 line will go to a logic "low" when address lines (not)BA4, (not)BA5, (not)BA6, (not)BA7, (not)BA8, (not)BA9, and (not)BA10 are all logic "low".

The (not)SW signal is used to select the memory map position of the relay outputs, the keyboard input, and the RAM memory configuration of the Alarm board. The SW signal is generated by switch S3, section C1. It is then inverted by IC 5Ed, forming the (not)SW line.

The memory map and RAM memory configuration is shown in the table below:

(not)SW logic "high"			
RAM	2800	through	2FEF
RELAY OUTPUTS	2FF8	through	2FFB
KEYBOARD INPUT	2FFF		
(not)SW logic "low"			
RAM	not available		
RELAY OUTPUTS	2FF0	through	2FF3
KEYBOARD INPUT	2FF7		

The A3A line is an altered address 3 line. It is generated by exclusive OR-ing (not)BA3 with (not)SW, using IC 5Ea. If (not)SW is "low", A3A will be logic "high" when (not)BA3 is logic "high". If (not)SW is "high", A3A will be logic "high" when (not)BA3 is logic "low".

The (not)EDB, Enable Data Buffer, line will be logic "low" whenever data is to be transfered to, or from, the Alarm board. The (not)EDB line controls the tri-state outputs of the bi-directional data buffer, 1A. The (not)EDB line is generated by the decoding circuitry consisting of 4Ca, 5Bb, 4Ea, 4Eb, 4Ec, and 4Fa.

The UA0 line is NORed with the (not)BA10 line by IC 4Ca. The resulting signal is NANDed with the A3A line and the inversion of the (not)BOARD line by NAND gate 4Eb. The (not)BOARD line is inverted by IC 4Cd.

The output of 4Ca is inverted by the exclusive OR gate 5Eb, then NANDed with the inversion of the (not)BOARD line and the (not)SW line by NAND gate 4Ec. The output of 4Ec is NANDed with the output of 4Eb by NAND gate 4Fa. The resulting signal is NANDed with the system clock BF1 by NAND gate 4Ea. The output of 4Ea is the (not)EDB signal.

The RAM enables, OENP(not) and 1ENP(not), are generated by ICs 4Cc, 4Da, 4Db, and 5Db, along with Q1, Q2, Q3 and their associated circuitry.

The UA0 line is inverted by inverter 5Db, then NORed with (not)BA10 by NOR gate 4Cc. The resulting signal is NANDed with the system clock, BF1, and the inversion of (not)BOARD by NAND gate 4Db. The output of 4Db acts as the current sink for transistor Q2, which generates RAM enable OENP(not).

The (not)BA10 address line is NANDed with the system clock, BF1, and the inversion of (not)BOARD by NAND gate 4Da. The output of 4Da acts as the current sink for transistor Q1, which generates RAM enable 1ENP(not).

As long as the (not)BRESET line is a logic "high", the RAM enables will track the output of their respective driver, 4Da or 4Db. If the (not)BRESET line goes to a logic "low", the RAM enables, OENP(not) and 1ENP(not), will go to a logic "high" and remain there until (not)BRESET returns to a logic "high".

The output data register strobes, CK0 through CK3, are used to select which of the four output data registers (refer to OUTPUT REGISTERS AND OPTO-ISOLATORS) is to be written to. The strobes are generated by IC's 3C and 3D.

Address lines (not)BA0, (not)BA1, and (not)BA2 are used as select inputs to the 1-of-8 decoder, IC 3C. The (not)BOARD line acts as one logic "low" enable to 3C and the UA0 line acts as the other logic "low" enable. The A3A line acts as the logic "high" enable for 3C.

When (not)BOARD and UA0 are both logic "low" in conjunction with A3A being logic "high", the output of 3C, as selected by the (not)BA0, (not)BA1, and (not)BA2 address lines, will be enabled. The selected output will go to a logic "low". The output-data-register select lines come out on the Y4, Y5, Y6, or Y7 outputs of 3C.

The Y7 output is NORed with the BR/(not)W signal, by IC 3Da, to generate output-data-register strobe CK0. The Y6 output is NORed with the BR/(not)W signal, by IC 3Db, to generate output-data-register strobe CK1. The Y5 output is NORed with the BR/(not)W signal, by IC 3Dc, to generate output-data-register strobe CK2. The Y4 output is NORed with the BR/(not)W signal, by IC 3Dd, to generate output-data-register strobe CK3.

The Y0 output of 3C is used by the input data control system to generate the RDKY(not) line (refer to INPUT DATA SYSTEM AND CONTROL).

2.4.2.3 Timing Circuits

The system clocks, BF1 and BF1x8, are used by IC 5C to generate a precessed clock. This clock is NANDed with the BR/(not)W signal by NAND gate 4Fc to form the @M clock.

2.4.2.4 RAM

The Alarm board has provisions for 2K bytes of memory, using type 4334-3 (1K x 4) RAMs, to provide storage for the alarm set points. Buffered address lines (not)BA0 through (not)BA9 are used to address the RAMs.

The RAMs are paired into two 1K words x 8 bit blocks with one RAM of each pair storing the upper four bits, and the other RAM storing the lower four bits of each 8-bit byte.

The buffered data lines, BD0 through BD3, go to the RAMs, 2D and 2E, which store the lower 4 bits of the data, while the buffered data lines BD4 through BD7 go to the RAMs, 2B and 2C, which store the upper 4 bits of the data.

The lower 1K x 8 memory block (2C and 2E) is enabled by the OENP(not) control signal originating in the DECODING section.

The upper 1K x 8 memory block (2B and 2D) is enabled by the 1ENP(not) control signal from the DECODING section.

The buffered address and data lines which go to the RAMs are pulled up by 10Kohm resistors to the +5VI voltage source, which is two diode-drops below the +5 volt supply. The two diode-drops are used to insure that the logic level on the data or address lines does not exceed the supply voltage specification for the RAMs.

The RAM memories are provided with a battery back-up system which will preserve the contents of the memories in the event of a power failure, or if the power to the unit is turned off.

The Alarm board may be removed from the unit without the loss of the RAM memory contents. The change-over from the system power to the battery power, and from the battery power to the system power, is automatic.

2.4.2.5 Output Registers and Opto-isolators

The Alarm board is designed to drive two Relay panels with each Relay panel having provisions for 16 relays. There are two separate output sections, each having two 8-bit output data registers and eight dual opto-isolators.

The two 8-bit output data registers, 3H and 4H, along with the eight dual opto-isolators, 3KA, 3KB, 3LA, 3LB, 4KA, 4KB, 4LA, and 4LB, and NAND gates 3Eb and 3Ed make up output section A.

The two 8-bit output data registers, 1H and 2H, along with the eight dual opto-isolators, 1KA, 1KB, 1LA, 1LB, 2KA, 2KB, 2LA, and 2LB, and NAND gates 3Ea and 3Ec make up output section B.

The output-data-register strobes, CK0 - CK3, are used to strobe the output data into the respective output register. The output strobes are NANDed with the precessed clock, @m. The output registers hold the data being sent to the relay board via the opto-isolators.

The resistor networks, RN4 - RN7, act as current limiting resistors for the LED (Light Emitting Diodes) in the opto-isolators. The outputs of the section

A opto-isolators are interfaced to the external Relay panel via connector J2. The outputs of the section B opto-isolators are interfaced to the external Relay panel via connector J1.

2.4.2.6 Input Data System and Control

The data coming from the Relay panels is buffered by opto-isolators and then passed through tri-state drivers onto the onboard input data bus.

The keyboard strobes coming from the Relay panels are sent to an arbitration circuit which will decide which keyboard's input data will be enabled onto the input data bus, and then strobed into the input data register.

Opto-isolator 1MB buffers the data STROBE(not) and data STROBE ENable coming from Relay panel B.

Opto-isolators 1MA and 2MB buffer the data coming from relay panel B.

Opto-isolator 2MA buffers the data STROBE(not) and data STROBE ENable coming from Relay panel A.

Opto-isolators 3MA and 3MB buffer the data coming from relay panel A.

To prevent noise on the interface cable, between the Alarm board and the Relay panel, from getting into the Alarm board's input data system, the outputs of the opto-isolators are fed into schmitt-trigger inverters.

The received data is buffered by a tri-state buffer, 5J, onto the onboard input data bus. The data is then strobed into the data register, 5H, under the control of the keyboard arbitrator circuitry, for transfer to the system bus through the system bus driver 1A.

The keyboard arbitrator circuit decides the order in which the Relay panel's keyboard input data is read by the Alarm board. The keyboard arbitrator consists of IC's 5K, 5L, 5M, and 5N.

If the keyboard input data from Relay panel B, J1, should become active, the STROBE EN signal will be logic "high" and STROBE(not) will go to a logic "low" state. These two signals are buffered by opto-isolator 1MB. The logic "high" STROBE EN signal will cause the output of the schmitt-trigger inverter 4Nf to be logic "low". The logic "low" STROBE(not) signal will cause the output of the schmitt-trigger inverter 4Nd to be a logic "high". The output of 4Nd is then inverted by IC 5Nd. The output signals from 5Nd and 4Nf are then NORed together by NOR gate 5Nb.

When the STROBE EN signal is logic "high", and the STROBE(not) signal is pulsed to a logic "low", the output of NOR gate 5Nb will go to a logic "high" for the duration of the logic "low" state of the STROBE(not) signal. This transistion will clock the Q output, the PR4 line, of flip-flop 5Lb to a logic "low".

The PR4 line is connected to one input, pin 13, of NAND gate 5Md. A logic "low" on the PR4 line will act as an inhibit control to the input circuitry for the A Relay panel, and prevent the inputting of data from the A Relay panel until the CPU has serviced the B Relay panel's keyboard input.

When the Q output of flip-flop 5Lb goes to a logic "low", its Q(bar) output will go to a logic "high".

If the A Relay panel's keyboard is not currently being serviced, flip-flop 5Ka will be set on the next positive transistion of the system clock BF1. When flip-flop 5Ka is set, its Q output, the R4 line, will go to a logic "high", and its Q(bar), the S1 line, will got to a logic "low".

The R4 line acts as the data buffer enable for the A Relay panel, and the S1

line acts as the data buffer enable for the B Relay panel. A logic "high" on the R4 line will disable the A Relay panel's data buffer 5Ja. The logic "low" on the S1 line will enable the B Relay panel's data buffer, 5Jb. Data buffer 5Jb will then drive the B Relay panel's data DI0(not)-DI3(not) onto the R0-R3 lines of the internal data bus.

The S1 line is connected to one input, pin 10, of NAND gate 5Mc. When S1 goes "low" the DRDY, data ready, line will go to a logic "high". If the system is not in a RESET mode, this positive transistion of DRDY will clock flip-flop 5Ba, setting its Q output to a logic "high". On the next positive transistion of the system clock, BF1, the Q output of flip-flop 5Bb will be clocked "high", causing the interrupt request, BIRQ, line to go "high".

The BIRQ line drives the base of transistor Q6 through resistor R4. When the BIRQ line is "high", Q6 is turned ON and will place a logic "low" on the system's (not)IRQ line.

The positive transition of the BIRQ line will latch the keyboard input data into the tri-state register IC 5H. S1 is also latched into 5H to indicate to the CPU which Relay panel is being serviced. In addition, two inputs to 5H are supplied by switch S3, sections C2 and C3. These inputs select the ISA configuration code for the Alarm board.

NOTE

> To insure that the ISA configuration code, selected by switches S3C2 and S3C3, is properly read by the CPU upon power up, both flip-flops 5Ba and 5Bb are preset during the system reset cycle. To accomplish this, the preset inputs of both flip-flops are connected to the (not)BRESET line, which goes to a logic "low" during all reset cycles. This will cause the BIRQ line to be set to a logic "high" following any system reset. Thus the ISA code will be latched into the input data register, IC 5H, so that the CPU can read it, following power up.

When the CPU responds to the IRQ and reads the Alarm board's keyboard data input, the address of the board's keyboard input will be decoded by the decoding section (refer to DECODING CIRCUITS).

When the keyboard input is addressed, the Y0 output of IC 3C will go to a logic "low". This signal is inverted by inverter IC 5Da. The output of 5Da is NANDed with the BR/(not)W and BF1 signals by NAND gate 4Fb.

The output of 4Fb is the RDKY(not), Read Keyboard, line. The RDKY(not) line will be clocked to a logic "low" in sync with the BR/(not)W and BF1 signals.

A logic "low" on the RDKY(not) line will enable the tri-state outputs of the input data register, IC 5H, onto the data bus.

The keyboard input data R0-R3 will be driven onto bits BD0-BD3 of the data bus.

The Relay panel select line S1 is driven onto data bit BD4 of the data bus.

The ISA configuration code is driven onto data bits BD5 and BD6 of the data bus.

The RDKY(not) line will also enable the output of the tri-state buffer gate 5Af, which will drive the BIRQ line onto data bit BD7 of the data bus.

The RDKY(not) signal is inverted by IC 5Nc to form the RDKY line. The RDKY line is NANDed with the R4 line by NAND gate 5Mb. The output of 5Mb will go

"low" when both RDKY and R4 are logic "high". A logic "low" on the output of 5Mb will preset the B input strobe flip-flop, 5Lb.

On the next positive transition of the system clock BF1, the second flip-flop, 5Ka, will be reset. This action will result in the removal of the DRDY signal. RDKY will also clear flip-flop 5Ba.

Flip-flop 5Bb will reset on the next positive transistion of the system clock BF1. This will cause the BIRQ line to return to a logic "low", causing transistor Q6 to turn OFF, allowing the system's (not)IRQ line to return to a logic "high".

In the case where the A Relay panel is inputting data and the B Relay panel is not, the same sequence of events takes place except that when the A input strobe flip-flop 5La is set, its Q output will go "low" and act as a clear input to flip-flop 5Ka.

With flip-flop 5Ka cleared, its Q(bar) output, the S1 line, will be a logic "high", and its Q output, the R4 line, will be a logic "low".

A logic "high" on the S1 line will disable the B Relay panel's data buffer 5Jb.

A logic "low" on the R4 line will enable the A Relay panel's data buffer 5Ja.

Data buffer 5Ja will then drive the A Relay panel's data DI0(not)-DI3(not) onto the R0-R3 data lines of the internal data bus.

Flip-flop 5Kb will be set on the next positive transistion of the system clock BF1. This will cause the Q(bar) output, the S0 line, of flip-flop 5Kb to go to a logic "low".

The S0 line is connected to one input, pin 9, of NAND gate 5Mc. When the S0 line goes to a logic "low", the output of NAND gate 5Mc, the DRDY line, will go to a logic "high".

When the CPU services the IRQ and reads the keyboard input data, as previously described, the RDKY signal generated is NANDed with S1, by NAND gate 5Ma, to preset flip-flop 5La.

On the next positive transistion of the system clock BF1, flip-flop 5Kb will be reset, and S0 will go "high", resulting in the removal of the DRDY signal.

2.4.3 Alarm Relay Panel, General

Assembly: 231-4370-00
Schematic: 231-6370-00

The Alarm Relay panel is a remote peripheral device for use with the Alarm Monitoring board. The panel contains 16 relays and their associated relay driver circuitry. In addition, the panel has the necessary circuitry to encode up to 20 keys.

The Relay panel is driven by the Alarm board located in the 235. Up to two Relay panels can be supported by an Alarm board.

The Relay panel contains its own power supply, which powers both the Relay panel and the interface opto-isolators located on the driving Alarm board.

The Relay panel can be broken down into three main sections:

1. RELAYS AND RELAY DRIVER CIRCUITS
2. KEYBOARD ENCODER
3. POWER SUPPLY

2.4.3.1 Relays and Relay Driver Circuits

There are 16 relays, K0-K15, on the Relay panel. Each relay has its own relay driver circuitry. The relay driver circuitry is driven, in turn, by the output of an opto-isolator located on the Alarm board. There is one opto-isolator for each relay.

The driving signals, RY0(not)-RY15(not), are interfaced to the Relay panel via connector J1. The driving signal for a particular relay is first conditioned by an RC filter network to prevent any noise picked up by the interconnecting cable from affecting the operation of the Relay panel.

The output of the conditioning circuit is applied as the input to a 74C14 CMOS schmitt-trigger inverter (Z12, Z14, and Z16). The output of the schmitt-trigger is used to drive the relay driver made up from one section of a ULN2003A (Z13, Z15, and Z17). The output of the ULN2003A drives the relay (K0 - K15). The relay coil is shunted by a 1N914 diode to protect the driver from the current spike generated when the relay coil is de-energized.

Each relay has both normally open (NO) and normally closed (NC) contacts. The common of each relay is connected to the appropriate position on terminal strip TB5. The "NO" contact of each relay is connected to the appropriate position on terminal strip TB6. The "NC" contact of each relay is connected to the appropriate position on terminal strip TB4.

2.4.3.2 Keyboard Encoder

The Relay panel has the necessary circuitry to encode 20 keys. However, only the first 16 keys are used. The keys may be any form of SPST momentary switch that is normally open. The encoded data is sent via connector J1 to the Alarm board located in the Digitrend 235.

IC Z1 is a free-running oscillator which acts as the master clock source for the encoder circuitry. The output of Z1 is connected to the two NAND gates Z2a and Z2b. NAND gate Z2a is wired as an inverter. Its output drives the CLK line, which is the master clock line for the encoder circuitry. The second input to NAND gate Z2b is the (not)LATCH signal which, is generated by the encoder logic. The output of Z2b is the GCLK, Gated Clock, line which acts as the clock for the scan counter, IC Z7.

The scan counter, Z7, is an 8-stage binary counter of which only the first six stages are actively used. The counter is clocked by the negative transistion of the GCLK line. The SC output of Z7 is inverted by inverter Z8c to form (not)SC. The outputs, DA through DE, and SC, from Z7 along with (not)SC, are applied to the three 1-of-8 decoders (Z3, Z4, and Z5).

The outputs of the decoders form 20 discrete logic "low" going key strobe signals. Only one key strobe signal is logic "low" at a time. The eight outputs of Z5, and the lower two outputs of Z3, form the S0-S9 lines that are sent to terminal strip TB0. The upper six outputs of Z3, and the lower four outputs of Z4, form the 10-19 lines that are sent to terminal strip TB2.

Each terminal on TB0 can be wired to one side of a momentary, normally open, SPST switch. The other side of the switch is then wired to the appropriate terminal on terminal strip TB1. The same is true for TB2 and TB3.

When a switch is closed, scan counter Z7 is clocked to the point at which the corresponding decoded key strobe goes to a logic "low". At that time, the input diode in the opto-isolator, IC Z9, will turn ON. Its ON current will be

sunk to ground through the closed switch and the output driver in the corresponding decoder. The output of the opto-isolator will go to a logic "low". The output of the opto-isloator is inverted by inverter Z16f. Z16f is a 74C14 schmitt-trigger inverter which helps to insure a clean response to a switch closure.

When the output of the opto-isolator goes to a logic "low", the output of inverter Z16f will go to a logic "high". The output of Z16f is connected to the 4D input, pin 13, of the quad flip-flop, IC Z6. On the next positive transition of the CLK line, the fourth stage of Z6 will be set. The Q4(bar) output, pin 14, of Z6 will go "low", and cause the output of NAND gate Z2d, which drives the LATCH line, to go to a logic "high".

The LATCH line is connected to the clock input of the output data register, IC Z11. The positive transition of the LATCH line will latch the current output lines, DA-DE, of the scan counter, Z7, into the output data register, Z11. The outputs of Z11 drive inverters Z8a, Z8b, Z8d, Z8e, and Z8f, which act as buffers to drive the data onto the cable that connects the Relay panel to the Alarm board located in the Digitrend 235.

The latched and buffered DA-DD lines become the DI0(not)-DI3(not) lines, that are sent to the Alarm board in the Digitrend 235. The latched and buffered DE line becomes the STROBE EN line which is sent to the Alarm board. The LATCH line is inverted by inverter Z10f to drive the (not)LATCH line, which is used as the gating control by NAND gate Z2b in generating the GCLK line. This will cause the GCLK line to remain in the logic "high" state, and thus stop the scan counter, Z7.

The LATCH line is also connected to the 1D input, pin 4, of the quad flip-flop Z6, and to one input, pin 10, of NAND gate Z2c. The Q4 output, pin 15 of Z6, is connected to the 3D input, pin 12, of Z6.

On the next positive transition of the CLK line, the first and third stages of Z6 will be set. The Q1 output, pin 2 of Z6, will go to a logic "high", and the Q3(bar) output, pin 11 of Z6, will go to a logic "low". The Q1 output of Z6, pin 2, is the second input to NAND gate Z2c. When Q1 goes to a logic "high", the output of Z2c will go to a logic "low". This signal is connected to the 2D input of the quad flip-flop Z6.

On the next positive transition of the CLK line, the second stage of Z6 will be reset and the Q2(bar) output, pin 6 of Z6, will go to a logic "high". The Q2(bar) output of Z6 is inverted by inverter Z10a. Inverter Z10a acts as a buffer to drive the data STROBE(not) signal onto the external cable that connects the Relay panel to the Alarm board in the Digitrend 235.

When the switch is opened, the input diode of the opto-isolator Z9 will turn OFF, and its output will go to a logic "high", pulled up to +5 volts by resistor R7. This will cause the output of Z16f and thus the 4D input to Z6 to be "low".

On the next positive transition of the CLK line the fourth stage of Z6 will be reset. This will cause the Q4 output to go to a logic "low", and the Q4(bar) output to go to a logic "high". With the Q4 output logic "low", the 3D input is also logic "low".

On the next positive transition of the CLK line, the third stage of Z6 will be reset, and it's Q3(bar) output will go to a logic "high". When both Q3(bar) and Q4(bar) are logic "high", the output of NAND gate Z2d, the LATCH line, will go to a logic "low" that will enable the GCLK line through the operation of NAND gate Z2b. The logic "low" on the LATCH line will also cause the output of Z2c to go to a logic "high" and thus the 2D input of Z6 will be a logic "high".

On the next positive transition of the CLK line, the second stage of Z6 will be set, and the Q2(bar) output of Z6 will go to a logic "high". This will cause the output of inverter Z10a to go to a logic "low", and thus remove the STROBE(not) signal going to the Alarm board in the Digitrend 235. Also, the first stage of Z6 wil be reset, causing the Q1 output to go to a logic "low".

The keyboard encoder circuitry is now ready to service the next switch closure.

2.4.3.3 Power Supply

The power supply provides +24 volts for the relays and +5 volts for the digital logic devices on the Relay panel. In addition, the +5 volts produced on the Relay panel is also sent, via connector J1, to the Alarm board, to power the keyboard input data opto-isolators.

The power supply consists of transformer T1, rectifiers CR18 through CR21, filter capacitor C23, and regulator Z18.

The output of the secondary winding of T1 is applied to the full-wave bridge rectifier, CR18 through CR21. The DC voltage from the bridge rectifier is filtered by capacitor C23 and is approximately 24 volts. The filtered 24 volts is used to power the relay coils.

The filtered 24 volts is also applied to the input of regulator IC Z18. The output of Z18 is a regulated +5 volt, used to power the digital devices on the Relay panel, and the opto-isolators located on the Digitrend 235 Alarm board. Regulator Z18 is mounted on a heat sink to help dissipate the heat produced by the device.

As an alternate power source, a 24 volt battery may be connected to the Relay panel by connecting the battery terminals to TB7. A diode is be used to isolate the battery from the main power supply.

2.4.4 Serial I/O Port #2 Board, General

Assembly: 231-4470-00
Schematic: 231-6470-00

The main function of the Serial I/O Port #2 board is to provide a second serial interface to support a communication link between the Digitrend 235 and an external device. The interface will support both RS-232 and 20 mA current loop data links at the following baud rates:

9600 BAUD
4800 BAUD
2400 BAUD
1800 BAUD
1200 BAUD
600 BAUD
300 BAUD
110 BAUD

In addition to the serial interface circuitry, the board also has provisions for an optional 128-byte software configuration PROM and 256-bytes of optional

RAM. The optional RAM is normally not used, so it is deselected to prevent possible bus contention problems.

In the current configuration of the Serial I/O board, for use in the Digitrend 235, the optional PROM and RAM are not used. These ICs, the RAM (1B) and the PROM (1C), are not installed in the basic Digitrend 235 Serial I/O board.

The memory space allocated to the Serial I/O board is from 2000 to 21FF. The memory map of the Serial I/O board within this allocated space is as follows:

2000 - 20FF	Optional RAM memory space
2100 - 217F	Optional configuration PROM memory space
21C0	ACIA control/status address
21C1	ACIA input/output data address

The Serial I/O board can be divided into seven functional sections:

1. BUFFERS
2. DECODING CIRCUITS
3. RAM AND PROM
4. BAUD RATE GENERATOR
5. ACIA
6. SERIAL LINE DRIVERS/RECEIVERS
7. ISOLATED POWER SUPPLY

2.4.4.1 Buffers

All data, address, and control signals coming from the system bus onto the Serial I/O board, or from the Serial I/O board onto the system bus, are buffered.

The data lines are buffered by a bi-directional bus driver, 1A. The direction of data flow is determined by the system R/W line. The R/W line is inverted by inverter 2Ec. The output of 2Ec is used as the direction control for the bi-directional data buffer 1A.

When the system R/W line is logic "high", the board is in the read mode and the flow of data is from the Serial I/O board onto the system bus.

When the system R/W line is logic "low", the board is in the write mode and the flow of data is from the system bus onto the Serial I/O board.

The tri-state outputs of the data buffer are controlled by the data bus enable, (not)DBE, line generated by the decoding circuitry (refer to DECODING).

The address lines are buffered by ICs 2A and 3A. 2A buffers the lower eight address lines, A0-A7, while 3A buffers the upper eight address lines, A8-A15. These buffers are wired to keep their tri-state outputs always enabled.

The system clock line, F1, is buffered by 2Bb, to drive the BF1 line. 2Bb is a non-inverting tri-state buffer with its enable input wired to ground to keep its output enabled.

The R/W line is not only buffered by 2Ec, as described above, but it is also buffered by 2Bd, to drive the BR/(not)W line. 2Bd is a non-inverting tri-state buffer with its enable input wired to ground to keep its output enabled.

The system (not)VMA line is loaded by one input, pin 2, of NOR gate 2Da in the decoding circuitry (refer to DECODING CIRCUITS).

The system (not)IRQ line is driven by the ACIA (refer to ACIA), through the tri-state buffer 2Ba. The input of 2Ba is wired to ground and the (not)BIRQ

line, driven by the ACIA, is used as the enable input.

All incoming signal lines are loaded by only one low power schottky TTL load, except R/W which has an additional LS TTL load.

2.4.4.2 Decoding Circuits

The board and address decoding is performed by ICs 1Ea, 2Ca, 2Cb, 2Cc, 2Da, 2Db, 2Dd, and 2Ea. The board is designed to function in the memory space from 2000 to 21FF.

However, since the RAM located from 2000 to 20FF is normally deselected, the address line BA8 is fed into one input, pin 2, of NAND gate 1Ea to disable the decoding section during any accesses to this memory area.

If the RAM is to be used, the BA8 clad trace on the board going to 1Ea, pin 2, must be cut. The 4.7K resistor R6 will then hold this input logic "high", enabling the decoding section during any accesses to this memory area. This disable function will prevent the data bus driver 1A from being turned on during any accesses to the RAM space, if the RAM is not to be used. This prevents any bus contention problems if any other boards in the system should attempt to use the memory space from 2000 to 20FF.

The second input, pin 1, of 1Ea is connected to address line BA13. When BA13 and BA8 are both logic "high", the output of 1Ea will be logic "low". This signal is NORed with the address lines BA14 and BA15 by the three input NOR gate, 2Cb. When BA14 and BA15 are logic "low" in conjunction with the logic "LOW" output of 1Ea, the output of 2Cb will be logic "high". Address lines BA10, BA11, and BA12 are NORed together by the three input NOR gate, 2Cc. When BA10, BA11, and BA12 are all logic "low", the output of 2Cc will be logic "high". The output of 2Cc is NANDed with the output of 2Cb by NAND gate 2Da. When the outputs of both 2Cb and 2Cc are logic "high", the output of 2Da will be logic "low".

The output of 2Da is NORed with the system (not)VMA line and with address line BA9 by the three input NOR gate 2Ca. When the output of NAND gate 2Da, the (not)VMA line, and address line BA9 are all logic "low", the output of 2Ca, which drives the BS (Board Select) line, will go to a logic "high".

The BS line is used as a chip select by the RAM memory (refer to RAM AND PROM). The BS line is inverted by inverter 2Ea to drive the (not)BS line that is used to control the +5 volts for the PROM. The BS line is NANDed with the BA8 address line by NAND gate 2Dd. The output of 2Dd drives the (not)SEL line. When the BS line and address line BA8 are both logic "high", the (not)SEL line will go to a logic "low". The (not)SEL line is used as a chip select for the PROM, and as a chip select for the ACIA (refer to ACIA).

The BS line is NANDed with the BF1 line by NAND gate 2Db. The output of 2Db drives the (not)DBE line, which is used to enable the tri-state outputs of the bi-directional data buffer 1A (refer to BUFFERS). When the BS and BF1 lines are both logic "high", the output of 2Db will be logic "low". A logic "low" on the (not)DBE line will enable the tri-state outputs of the data buffer 1A.

The system R/W line is inverted by inverter 2Ec. The output of 2Ec is NANDed with the BF1 line by NAND gate 2Dc. The output of 2Dc drives the RAM R/W line, which acts as the read/write control for the optional RAM memory.

2.4.4.3 RAM and PROM

The RAM function is supplied by 1B (if used), and the PROM function is supplied by 1C (if used). The RAM, 1B, is addressed by address lines BA0-BA7. Address line BA8 is used as a logic "low" chip select. The BS line is used as a logic "high" chip select. The BR/(not)W line is used to control the tri-state outputs of the RAM memory. When the BR/(not)W line is logic "low", the tri-state outputs are disabled, so the shared I/O pins of the device can act as data inputs to allow data to be written into the RAM. When the BR/(not)W line is logic "high", the tri-state outputs are enabled to allow data to be read from the RAM. The RAM R/W line is used to control the writing of data into the RAM.

When the RAM is selected, by having a logic "low" on the BA8 address line and a logic "high" on the BS line, and the BR/(not)W line is logic "low", a logic "low" pulse on the RAM R/W line will cause the data on the data lines, BD0-BD7, to be written into the RAM.

The PROM, 1C, is addressed by address lines BA0-BA6. Address line BA7 is used as a logic "low" chip select. The second logic "low" chip select input to the PROM is the (not)SEL line. When the (not)SEL line and address line BA7 are both logic "low", the PROM will be enabled.

Transistor Q3 acts as the +5 volt power switch for the PROM. When not addressed, the PROM is powered down to reduce power consumption and heat dissipation. When the PROM is addressed, the (not)BS line will be logic "low". A logic "low" level on the (not)BS line will bias transistor Q3 ON, supplying +5 volts for the PROM. When the PROM is not addressed, the (not)BS line will be logic "high", which will bias Q3 OFF, removing the +5 volts from the PROM.

2.4.4.4 Baud Rate Generator

Crystal Y1 and IC 4G form the baud rate generator. 4G provides multiple outputs, which are fed to the baud rate select switch S2. The selected baud rate is applied to ACIA 1D transmit and receive clock inputs, pins 3 and 4.

2.4.4.5 ACIA

IC 1D is the Asynchronous Communications Interface Adapter (ACIA). The ACIA occupies two address locations in the Serial I/O board's allocated memory space. The control/status registers reside at 21c0, and the data I/O registers reside at 21c1.

Address lines BA6 and BA7 act as logic "high" chip select inputs to the ACIA. Address line BA0 acts as the register select input which determines which register set is to be accessed. When BA0 is logic "low", the control/status registers will be accessed. When BA0 is logic "high", the data I/O registers will be accessed.

The BF1 line acts as the clock input for the ACIA to sync it with the system. The read/write function of the ACIA is controlled by the BR/(not)W line. When the BR/(not)W line is logic "high", the ACIA is in the read mode. When the BR/(not)W line is logic "low", the ACIA is in the write mode.

The ACIA is selected when address lines BA6 and BA7 are both logic "high", in conjunction with the (not)SEL line being logic "low". Address line BA0 will

then select the active registers.

The data to be transmitted is written into the data transmit register. The ACIA then serializes the data and transmits it at the rate determined by the transmit clock frequency. The transmitted data, TXO, comes out of the ACIA on pin 6, and is double inverted by inverters 2Ed and 2Ee, to form BTXO, and is then sent to the SERIAL LINE DRIVERS/RECEIVERS circuitry. This double inversion increases the drive output capability of the ACIA's transmit output, while maintaining the same logic state.

The received serial data, RXO, which comes from the SERIAL LINE DRIVERS/RECEIVERS circuitry, is connected to pin 2 of the ACIA. The ACIA converts the serial data to parallel data, and stores it in the received data register. The received data may then be read by the system from the received data register. When data is received, the ACIA's (not)IRQ output, pin 7, will drive the (not)BIRQ line to a logic "low". This line is buffered onto the system's (not)IRQ line by the tri-state buffer 2Ba.

The receive and transmit clock inputs, pins 3 and 4 of 1D, are connected to the baud rate select switch, S2.

The ACIA has two control inputs, the (not)DCD line, pin 23, and the (not)CTS line, pin 24. Both of these lines come from the SERIAL LINE DRIVERS/RECEIVERS circuitry. The ACIA has one control output, the (not)RTS line, pin 5. These control inputs and outputs provide the handshake signals required to interface the Serial I/O board to a terminal or modem.

2.4.4.6 Serial Line Driver/Receiver: RS-232

The transmit data, BTXO, which is generated by the ACIA, is connected to the input of 1Ga. 1Ga is a RS-232 compatible line driver. The output of 1Ga drives the BB RECEIVED DATA line, pin 3, of the serial interface connector J1.

The BA TRANSMITTED DATA line, pin 2, of the serial interface connector J1 is connected to the input of 1Ha. 1Ha is a RS-232 compatible line receiver. If a RS-232 compatible line is not connected to pin 2 of J1, resistor R12, will bias the input of 1Ha so that its output is logic "low". The output of 1Ha is inverted by inverter 2Ef. The output of 2Ef is connected to one input ot NAND gate 1Ec. The other input to 1Ec is connected to the current loop receiver's output. If the current loop input is not used, the output of the current loop receiver is pulled to a logic "high" by resistor R3. The output of NAND gate 1Ec drives the RXO line which is the serial data input for the ACIA.

The CA REQUEST DATA line, pin 4 of the serial interface connector J1, is connected to the input of 1Hb. 1Hb is a RS-232 compatible line receiver. The output of 1Hb drives the (not)CTS line which is a control input to the ACIA. If no connection is made to the CA REQUEST DATA line, the output of 1Hb will be a logic "high" which will inhibit the operation of the ACIA. Therefore, if this input is not used, it should be tied to pin 9 of the serial interface connector J1.

The CD DATA TERMINAL READY line, pin 20 of the serial interface connector J1, is connected to the input of 1Hc. 1Hc is a RS-232 compatible line receiver. The output of 1Hc drives the (not)DCD line which is a control input to the ACIA. If no connection is made to the CD DATA TERMINAL READY line, the output of 1Hc will be a logic "high", which will inhibit the operation of the ACIA. Therefore, if this input is not used, it should be tied to pin 9 of the serial interface connector J1.

The (not)RTS line, which is generated by the ACIA, is connected to the input of 1Gb. 1Gb is a RS-232 compatible line driver. The output of 1Gb drives the CB CLEAR TO SEND line, pin 5; the CC DATA SET READY line, pin 6; and the CF CARRIER DETECT line, pin 8; of the serial interface connector J1.

2.4.4.7 Serial Line Driver/Receiver: 20 mA Current Loop

The LED in opto-isolator 3G is driven by the serial data transmit, BTXO, line. Resistor R7 acts as a current limiting resistor for the LED in 3G. Opto-isolator 3G provides isolation for the 20ma current loop output. The output of 3G drives the 20ma current loop driver circuitry consisting of transistor Q1, resistors R11 and R9, zener diode CR5 and bridge rectifier CR6. One leg of CR6's output is connected directly to pin 11 of the serial interface connector J1. The other output of CR6 is connected to switch S1B. S1B is wired to allow this output of CR6 to be connected directly to pin 25 of J1 in the passive mode of operation, or through the isolated power supply (refer to ISOLATED POWER SUPPLY), in the active mode of operation.

The 20ma current loop receiver circuitry consists of transistor Q2, resistors R1, R13, and R14, diode CR7, and bridge rectifier CR8. One leg of CR8's input is connected directly to pin 18 of the serial interface connector J1. The other input to CR8 is connected to switch S1A. S1A is wired to allow this input of CR8 to be connected directly to pin 17 of J1 in the passive mode of operation, or through the isolated power supply in the active mode of operation. The output of the receiver circuitry drives the LED in 2G. Opto-isolator 2G provides isolation for the 20ma current loop input. The output of 2G is connected to one input of NAND gate 1Ec, as previously described.

2.4.4.8 Isolated Power Supply

The 20ma current loop interface is provided with an isolated voltage source for use in the active mode.

Transformer T1, diodes CR1-CR4, capacitor C22, and resistor R8 form the isolated power supply for the 20ma current loop transmit and receive sections (refer to SERIAL LINE DRIVERS/RECEIVERS).

2.4.5 Digital Inputs Board, General

The Digital/Status board is designed to operate in three different user selectable modes:

Digital input mode, status mode, and events mode.

In the "Digital Input" mode, it enables reading data into the Digitrend 235 from an instrument equipped with a digital output feature. In this mode it provides a full handshake via the READY and BUSY lines for each eight bits of digital data.

In the "Status" mode, it can be used to read in the status of active or passive circuitry. Six isolated five volt power supplies are provided to support the passive devices.

In the "Events" mode, a change of state on any one of the 48 input lines will

cause an interrupt to be generated, signaling the Digitrend 235 software that an event has taken place.

The Digital/Status board can be functionally divided into the following sections:

1. INPUT FILTER
2. I/O ISOLATOR
3. LOGIC LEVEL CONTROL
4. PERIPHERAL INTERFACE
5. EVENTS TRIGGER DECODER
6. TIMING AND ADDRESS DECODERS
7. BUS BUFFERS
8. ISOLATED AUXILIARY POWER SUPPLIES

2.4.5.1 Input Filter

All external inputs to the Digital/Status board pass through RC filters where high frequency noise is removed. Each filter consists of a 2.2Kohm resister in series with the input signal, followed by a .01 microfarad capacitor connected to that signal's ground.

Resistor networks RN7 through RN12, along with R1, R5, R9, R13 R17 and R21, provide the necessary 2.2Kohm resistors, while capacitor networks CN1 through CN6, along with C2, C4, C8, C8, C10 and C12, provide the .01 microfarad capacitors.

2.4.5.2 I/O Isolators

Each external signal coming onto, or off of, the Digital/Status board is isolated from the Digitrend 235's digital power supply by the ILCT6 opto-isolators, Z33 through Z62.

All inputs are required to provide a sink current of 1.6 milliamperes in the "low" state, and no current in the "high" state. Corresponding voltages are 1.5 volts or lower for a "low", and 4 volts or higher (up to 15 volts) for a "high". Surge protection on each opto-isolator is provided by diodes CR7 through CR60.

Each BUSY output will drive one TTL load (1.6 milliamps) through transistors Q1 through Q6. These outputs are protected against overvoltage by the 5.6 volt zener diodes, CR1 through CR6.

2.4.5.3 Logic Level Control

Positive or negative logic levels are switch selectable for all of the external signals to and from the Digital/Status board. Each input signal is brought into one input of a CMOS exclusive OR buffer, 74C86. The second input to these buffers comes from the DIP switch, S2. Switch S2-7 selects the logic level of the READY input, while S2-8 selects the logic levels of the 48 digital inputs. With S2-7 in the OFF position, the 6.8Kohm pull up resister, R36, holds the second input to the six "READY" exclusive OR buffers at 5 volts. This causes the READY signals to be inverted before being passed on to the peripheral in-

terface. Likewise, switch S2-8 in the OFF position allows the 6.8Kohm pull up resister, R31, to hold the second input of the "digital" exclusive OR buffers at 5 volts. This will invert all 48 incoming digital signals. With switch S2-7 or S2-8 in the ON position, the second input to the "READY" or "digital" exclusive OR buffers is held at ground. This allows the incoming signals to pass on to the peripheral interface section unchanged.

Switch S2-6 controls the logic level of the BUSY output. With this switch in the OFF position, the 6.8Kohm pull up resister, R35, holds the second input of the "BUSY" exclusive OR buffers at 5 volts. This will invert all six BUSY outputs before they leave the board. With switch S2-6 in the ON position, the second input to the "BUSY" exclusive OR buffers is held at ground. This allows the BUSY signals to leave the board unchanged.

2.4.5.4 Peripheral Interface

The peripheral interface section consists of the three PIAs (Peripheral Interface Adapters) Z7, Z8 and Z9, and is the actual interface between the peripheral world and the microprocessor bus.

The three PIAs are configured as input devices, during the power on initialization sequence, by storing all zeroes into their data direction registers. The control registers are then initialized, and the settings of the MODE SELECT switch (S2-1, S2-2 and S2-5) are determined by reading the CB2 status flag in each PIAs control B register. Any further programming of the PIA is then done by the software.

Each PIA acts as two, 8-bit wide gates. Data present on the input to the PIA is gated onto the microprocessor's data bus whenever the processor performs a READ operation from the memory location assigned to one of the PIA peripheral data registers.

The PIA interrupt inputs, CA1 and CB1, on all three PIAs, are used as the handshake input (READY) in the BCD mode, while the handshake output (BUSY) is controlled by CA2 and CB2. Since no handshaking occurs in the "Status" or "Events" modes, CB1 on Z9 is used as the EVENTS TRIGGER input in the "Events" mode.

2.4.5.5 Events Trigger Decoder

The 48 digital input signals are also connected to six 74C30, eight input NAND gates (Z10 through Z12 and Z15 through Z17). In the "Events" mode, all inputs are required to be in the same state (open or closed) initially. Switch S2-8 is used to ensure a high level at the input to the NAND gates.

When there is a change of state (event), one or more of the NAND gate inputs will go to ground. This will cause one or more of the NAND gates to output a "high" instead of its initial "low". All of the NAND gate outputs are inverted by the 74C04 hex inverter, Z14. These are then fed into six inputs of another 74C30 eight input NAND gate. The remaining two inputs are tied directly to 5 volts. The output of this NAND gate is tied, via switch S2-3, to the CB1 input of PIA Z9. Thus, when an event occurs, this line will immediately go "high", causing the CB1 status flag in the control B register of PIA Z9 to be set.

2.4.5.6 Timing and Address Decoders

A Digitrend 235 may contain up to two Digital/Status boards, each responding to unique addresses within the microprocessor's memory space. Address bits A15 through A9 are the same for both board No.1 and board No.2.

These address lines are decoded by the 74LS27 three input NOR gates, Z3, and the 74LS10 three input NAND gates, Z5. The VMA line is connected to a 74LS04 hex inverter Z6, and is also used in the decoding. When a valid PIA address is asserted on the bus, the appropriate decoding takes place, and a Valid Board Address (VBA) signal, and a Data Bus F1 Enable (DBFE) signal, goes "high".

Address bits A8 through A5 are used to select the individual Digital/Status boards. These four lines are connected to the 74LS42 four-to-ten line decoder, Z2. Outputs one through six are connected to DIP switch S1.

With switches S1-1, S1-2 and S1-3 in the ON position, the board will respond to hex addresses 242X, 244X and 246X. With switches S1-4, S1-5 and S1-6 in the ON position, the board responds to hex addresses 248X, 24AX and 24CX. Outputs seven through nine are connected to DIP switch S3. This switch is only installed on certain maintenance test boards, and causes the board to respond to hex addresses 24EX, 250X and 252X. Each of the three switch selected outputs is connected to one of the chip select inputs on PIA Z7, Z8 or Z9.

The microprocessor clock is buffered by the 74LS04 hex buffers, Z6, producing two timing signals, IT and OB. The OB signal is connected to the enable (E) input of each PIA, while IT is connected to switch S2-1, S2-2 and S2-5, where it is used during the board initialization process.

2.4.5.7 Bus Buffers

The Digital/Status Board interfaces to the Digitrend 235 by means of the Motherboard bus, which is buffered by the 74LS245 octal bus transceiver, Z1. Read/write, reset and IRQ are buffered by the 74LS244 octal buffer, Z4, as are address lines A0 and A1. This board adds one 74LS load to the Digitrend 235 bus. All timing signals are in accordance with the Digitrend 235 bus timing specification.

2.4.5.8 Isolated Auxiliary Power Supplies

Six isolated, auxiliary power supplies are provided to support devices which operate in a passive mode. Phases 1 and 2 of the Digitrend 235 power supply drive the primary winding of transformers T1 and T2. Phases 1 and 2 are 15 KHz square-waves of opposite phase, with a voltage swing of approximately 12 volts (-6v to +6v).

The output of each transformer is half-wave rectified and filtered by diodes CR67 through CR72 and the 22 microfarad tantalum capacitors C13 through C18. Each secondary winding, along with its associated circuitry, provides one isolated supply of 5.5 volts (+ or - 10%) at 20 milliamperes. Over voltage protection is provided on each power supply by the 6.8 volt zener diodes CR61 through CR66.

SECTION 3
TROUBLESHOOTING

3.1 GENERAL

This section of the manual covers the troubleshooting procedures for the Digitrend 235. Emphasis is placed on fault isolation of individual printed circuit board assemblies to determine which board(s) caused the failure.

A systematic method of fault isolation is used by observing the symptoms and proceeding to a particular course of action; narrowing the possibilities until the discrepant board is found. Using this approach will allow the user to quickly determine the nature of the failure without the need for elaborate test facilities.

Only the main system boards (refer to 2.2) will be covered in detail by this section. However, references will be made to the effects of failures occuring in option boards or FEMs upon operation of the Digitrend 235 where applicable.

3.2 PRELIMINARY TROUBLESHOOTING

Before attempting to troubleshoot the instrument, first make sure the difficulty is actually due to a malfunction within the instrument and not due to improper control settings, signal connections, or power source problems. This is done by (a) inspecting the ac line cord connections, (b) checking the condition of the ac fuse, (c) making sure the front panel key switch is ON, (d) inspecting all input signal connections, and (e) re-programming the unit to ensure that no programming error exists.

3.3 SYSTEM SUPPORT TREE

When external causes are ruled out, the user has two primary approaches to locating the faulty circuit board. The user can either perform a board by board substitution (if substitute boards are available) until the problem is resolved, or follow the procedures set forth in this section to isolate the failure to a particular board. The latter method will allow the user to isolate the failure without requiring a complete set of spare boards.

The Digitrend 235 is based on a microprocessor and contains all basic elements of a full computer system. The interaction of each board within the system and the microprocessor can result in a variety of symptoms in the event one of the boards fail.

Before the user can isolate the problem down to a particular board, he must first have some understanding of the dependency of the various boards within the system upon each other. For that reason, the troubleshooting procedures set forth in this section are based upon a system support tree.

In order to facilitate the troubleshooting task of the Digitrend 235, the user should think of the instrument as a stack of boards, or blocks. The posi-

tion of each block in the stack is dictated by the function of the block and the way in which it relates to the other blocks. The man/machine interface items (displays, keyboard, printer, and audible beeper) form the blocks which reside at the top of the stack, while the power supply resides at the bottom of the stack.

Due to this relative structure, if any of the blocks below the audio-visual blocks fail, the audio-visual blocks will generally provide some form of abnormal operation which will not only alert the user to the system failure but can also supply clues that can help the user in determining the source of the failure.

Shown below is a chart showing the relative block level of the board assemblies in the Digitrend 235:

LEVEL	ASSEMBLY
4	FRONT PANEL BOARD
3	PERIPHERAL INTERFACE BOARD
3	MEMORY EXTENSION BOARD
3	OPTION BOARDS
3	FEMs
2	CENTRAL PROCESSOR BOARD
1	MOTHER BOARD
0	POWER SUPPLY MODULE

Based on the symptoms present and the relative order of dependency of the system blocks, courses of action are prescribed to isolate the cause of failure. As an example of this dependency, all system blocks are dependent upon the power supply module and thus are supported by it. All system blocks, except the power supply module, are dependent upon the central processor board and thus are supported by it while the central processor board is supported by the power supply module.

3.3.1 Power Supply Troubleshooting

(no power ON indicator/ no display/ no printer activity)

Shown below is a typical failure support tree for the power supply module:

POWER "ON" INDICATOR FAILURE

POWER "ON" LED
|
FRONT PANEL BOARD
|
PERIPHERAL INTERFACE ADAPTER BOARD
|
MOTHER BOARD
|
POWER SUPPLY MODULE

The power supply accepts the ac line voltage and produces the various regulated voltages required by the Digitrend 235. The voltages produced are +5 volts, +12 volts, and -12 volts along with two square wave power outputs (15 kHz).

All troubleshooting should begin by observing the POWER ON LED indicator on the front panel to tentatively verify that the power supply module is operational. If the system and the POWER ON LED do not turn on when the power/program switch is in either the "ON" or "PRGM" position. then the failure is linked to the power supply module or to the front panel board.

Measure the voltage of the +5 volt supply on the mother board. The measurement can be made on the power supply bus of the mother board between pin 1 (GND) and pin 2 (+5V). The voltage read should be between +4.75 and +5.5 volts. If the voltage read is within this range, the failure is either on the peripheral interface adapter board or on the front panel board.

If the supply voltage measured was not in the above range, try adjusting the voltage with the +5V adjust on the power supply module. If the supply can be adjusted to fall within the proper range, then re-evaluate the symptoms.

If the power supply can not be adjusted to a level within the proper range, or if there is no voltage output from the supply, it is probably the source of the failure. The user should then check out the power supply.

WARNING

Hazardous voltages exist in and around the power supply circuitry. Use extreme caution when testing voltages and connections on the power supply board.

First remove the power cord from the power supply. Next remove the line fuse and check to see if it is still good. If the fuse is blown, replace it. With the power cord removed and the key switch in the "OFF" position, remove the power supply grounding lug and remove the power supply from the card cage. Place the power supply board on a non-conducting surface and reconnect the power cord. Leave the interconnecting cable between the power supply and the front panel connected.

Turn the front panel power switch to the "ON" position. Measure the voltage between pin 23 (+5V) and pin 28 (GND). If the measured voltage is not within the allowable voltage range of +4.75 to +5.25 volts, adjust R7 for a value within this range. If R7 cannot be adjusted within the range, the supply is defective and must be repaired or replaced.

If the +5 volt supply output reads normally, then check the +12 and -12 volt supply outputs (refer to the power supply module schematic 231-6500-00 for the proper pin numbers). If the supply operates normally when out of the card cage, but does not operate when plugged in, there are two possible causes:

1. There is a short on one of the power busses.
2. The supply has been damaged and cannot supply the current levels required.

If an ohm meter is available, check for a shorts between the power busses and the ground busses. If a short is found, remove all circuit board assemblies within the Digitrend 235, one board at a time until the short is removed. If the short is still present after removing the last board, the short is some-

where on the motherboard. The motherboard should then be repaired or replaced.

If an ohm meter is not available, then make sure that the front panel power switch is turned to the "OFF" postion and remove the power cord from the power supply board. Next, plug the power supply back into the card cage and reconnect the power cord. Turn the power switch to the "ON" position and check the power supply output voltages, mainly the +5 volt bus. If one of more of the supply voltages is still shorted to a low level, turn the supply OFF and remove all circuit board assemblies, one board at a time, starting with the FEMs. After removing a board, turn the supply ON and check the voltage levels again.

NOTE

> When performing this check-out procedure, always turn the power supply OFF before removing or replacing a board assembly.

If the short is still present, turn the supply OFF and plug the board back in and then remove the next board. Repeat this procedure until either the board causing the short condition is located, or until all boards have been checked.

If after all of the boards have been removed, one at a time, and the short has still not been located, unplug all of the boards except the power supply board. Turn the supply ON and check the voltages. If one or more of the supply voltages still read low and the power supply had previously checked out good when out of the card cage, then the short is on the motherboard. The motherboard should then be repaired or replaced.

3.3.2 CPU Board Troubleshooting

The CPU board is the functional center of the Digitrend 235, all the other boards in the system, except the power supply, are dependent upon it. If the data logger resets for unknown reasons, fails to run for even a limited period of time, or fails to run at all, the CPU board should be checked.

To determine if the problem is in the CPU board, first make sure that the front panel power switch is in the "OFF" position. Then remove all FEMs and option boards from the card cage.

NOTE

> If the main system software resides on a memory extension board, that board must be left plugged in.

In this stripped down form, turn the power ON and check to see if the Digitrend 235 is operational. If the data logger still fails to operate, the problem is probably on the CPU board, or on the memory extension board, if one is used. These boards should be swapped to determine which has failed.

3.3.3 PIA Board Troubleshooting

The PIA board forms the major interface link between the central processor (CPU), and the front panel board and FEMs. Through its interaction with the

front panel board it supports all of the man/machine interfaces, the displays, keyboard, printer, and buzzer. The PIA board also acts as the interface through which all communication between the central processor and the FEMs takes place. The PIA board also supports the watch dog circuitry which monitors the operation of the Digitrend 235.

A failure in the operation of the PIA board can result in a failure appearing in the display, the keyboard, the buzzer, the printer, the FEMs, or the watch dog system.

3.3.1.1 Display

Shown below is a typical failure support tree for the display:

```
DISPLAY FAILURE

      DISPLAY
         |
FRONT PANEL BOARD
         |
     PIA BOARD
         |
   MOTHER BOARD
         |
     CPU BOARD
```

Turn the front panel power switch to the "ON" position and press the "PAPER" key. All segments of the displays should light. If an individual display or an individual segment within an individual display fails to light, there is a problem on the front panel board and it should be repaired or replaced. If all numeric displays have the same segment failure, short pin 7 of IC 2A on the front panel board to the appropriate pin on IC 2H on the PIA board. See table below.

IC 2H PIN	SEGMENT
1	a
2	b
3	c
4	d
5	e
6	f
7	g
8	dec. pt.

If the segment in question fails to light during this test, the front panel board should be repaired or replaced. If the segment does light during this test, the PIA board should be repaired or replaced. If the segment did not light during this test, and replacement of the front panel board did not correct the problem, the interconnecting cable between the PIA board and the front panel board should be replaced. If this action does not correct the problem, the cause of failure may be on the CPU board.

If, when pressing the "PAPER" key, only one display is lit, and paper does not advance, the front panel board, interconnecting cable, and the PIA board should be replaced in that order until normal display operation is restored. If normal display operation is not restored after replacement of these items, the CPU board and power supply should then be checked for proper operation.

If all displays light and paper advances when the "PAPER" key is pressed, then press the "CLEAR" key and observe that all numeric displays are extinguished. If any display or individual segment of a display remains lit, there is a problem with the front panel board and it should be replaced. If replacement of the front panel board fails to correct the problem, then the CPU board should be checked.

If the display responds correctly to the above tests, but is dim in appearance, the +5VL supply from the power supply should be checked. If the +5VL supply is below +5 volts, the power supply should be checked or replaced. If the +5VL supply is at +5 volts then verify that, when the Digitrend 235 is displaying the CLOCK function, the seconds digits of the clock display advance at a 1Hz rate. If the clock operates normally, then the front panel board and the interconnecting cable should be checked and replaced as required. If the clock fails to operate normally, first the PIA board, and then the power supply should be checked and replaced if required. If no problems are found with the PIA board or the power supply, the CPU board should be checked.

3.3.1.2 Keyboard

Shown below is a typical failure support tree for the keyboard:

```
KEYBOARD FAILURE

    KEYBOARD
       |
FRONT PANEL BOARD
       |
    PIA BOARD
       |
  MOTHER BOARD
       |
    CPU BOARD
```

In order to properly diagnose a failure on the keyboard, it will be necessary to first press the "CLEAR" key followed by one of the other keys on the keyboard. The display should respond accordingly to the key being pressed (i.e. pressing "PRGM" results in "P" being displayed). This sequence is repeated for each key on the keyboard. The sequence should be performed in rows of keys on the keyboard. It should be noted which key(s) if any are not functioning when this test sequence is performed.

If an entire row of keys are inoperable, the problem can exist on the front panel board, the PIA board, or the keyboard itself. To test for the source of the failure, a jumper should be placed across the appropriate pins of IC 2A (a 4010) on the front panel board per the table below, and the function of that row re-tested. Shown below is the jumper connections required for testing each row:

JUMPER CONNECTIONS FOR IC 2A

KEY	PIN	CONNECTS TO PIN
CLEAR	3	2
PRGM	15	14
CALIB	12	11
RESET	10	9

If a given row of keys is still inoperable, the problem is either on the PIA board or the keyboard itself. The PIA board should be tested and replaced if necessary before any attempt is made to replace the keyboard. If the row of keys operate normally with the jumper on IC 2A, then replace the front panel board.

If a given column of keys are inoperable, then the problem is on the front panel board and it should be replaced. If only one key is inoperable, then the problem is probably on the keyboard itself and it should be inspected and replaced if required.

If replacement of the appropriate boards, as outline above, does not correct the keyboard failure, then the failure may be in the CPU board. The CPU board should be checked and replaced if required.

3.3.1.3 Buzzer

Shown below is a typical failure support tree for the buzzer:

BEEPER FAILURE

BEEPER
|
FRONT PANEL BOARD
|
PIA BOARD
|
MOTHER BOARD
|
CPU BOARD

If the buzzer fails to operate when a key is pressed or on power ON/OFF cycles, a failure may exist on either the front panel board or on the PIA board. Use a screw driver and adjust pot R44 on the front panel board while repeatedly pressing the "CLEAR" key. If the buzzer can be adjusted to an acceptable level, the buzzer is alright. If pot R44 has no effect, attach a jumper to pin 9 of IC 1E on the front panel board. Then alternately connect the other end of the jumper to pin 8 and pin 16 of IC 1E. If the beeper is operable it should beep. If it beeps during this test, the problem is probably on the PIA board and it should be replaced. If the buzzer fails the test then the front panel board is the source of the problem and it should be replaced.

If a buzzer problem is occuring in coincidence with a keyboard problem, correct the keyboard problem first.

3.3.1.4 Printer

Shown below is a typical failure support tree for the printer:

```
                    PRINTER FAILURE

PRINTER (PRINT HEAD & MOTOR ADVANCE)
                    |
            FRONT PANEL BOARD
                    |
                PIA BOARD
                    |
              MOTHER BOARD
                    |
                CPU BOARD
```

Problems with the printer on the Digitrend 235 can arise from four places, the printer motor, the print head, the front panel board, and the PIA board. The printer interconnect cable should be inspected first when the printer shows any problems in operation.

The printer normally prints 12 digits across the width of the paper with each digit being 5 segments wide and 7 segments high. If only one or two segments are out on the print head (i.e. not printing) then the print head should be replaced. If the same segment in each digit position is out, then the front panel board should be checked and replaced if required. If a single digit fails to print, then the front panel board and PIA board in that order should be checked and/or replaced.

SECTION 4
DRAWINGS AND PARTS LIST

4.1 GENERAL

Contained within this section are all drawings and parts lists for the various assemblies which comprise the Digitrend 235 data logger system. Schematic diagrams, a PCB top assembly drawing, and a parts list are provided for each printed circuit board assembly used in the Digitrend 235. In addition, wire lists for interface cables used with the Alarm Monitoring and Digital Inputs Board are also provided.

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, MAIN BOARD	MODEL NO. 235	DATE 2-27-80	SHEET 3 OF 3

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, MAIN BOARD	231-2300-00	1	
2	SCHEMATIC	231-6300-00	1	
3	TEST SPEC		1	
4				
5				
6	CONN, PC 56 AMP. 3-53066602	973-010-107	6	J1-J5,J11
7	CONN, PC 6 VIKING 2VH6/1AK12	973-010-51	5	J6-J10
8	CONN, PC 50 RIBBON (3M3433-2203)	973-060-10	1	P2
9	CONN, 40 P .1 CTR 1-87334-8	973-010-121	2	J12,J13
10	TERM STICK 8M (65611-108) BERG	973-381-01	1	P1
11	STDF, 7/16 X 440A3	991-020-01	3	

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, CPU	MODEL NO. 235	231-4340-01	D
		DATE 2-28-80	SHEET 3 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB CPU	231-2340-00	1	
2	SCHEMATIC	231-6340-00	1	
3	TEST SPEC			
4				
5				
6	IC, 74LS04 HEX INV(FC,MO,NL)	965-635-00	2	1F,2P
7	MAIN PROGRAM PATCH EPROM	231-7054-00	1	4H
8	IC, 74LS244 8 3-ST DRV(AMD,SIG	965-635-03	2	3M,4M
9	IC, 74LS245 8 BUS XCVR(TI,FC)	965-635-04	4	1A,2A,3A,3K
10	IC, 74LS175 QUAD 'D' FF	965-635-46	1	3N
11	IC, 74LS10 3-3IN NAND(TI)	965-635-08	2	3I,3J
12	IC, 74LS02 QUAD 2 IN NOR	965-635-17	4	1G,1I,2G,2I
13	IC, 74LS138 3-8 DEC/MUX	965-635-22	1	3G
14	IC, 74LS00 4-2 IN NAND(TI)	965-635-07	4	2C,2F,2J,4P
15	IC, 74LS86 4-2 IN EXCL OR	965-635-32	1	1J
16	IC, 74LS27 3-3IN POS-NOR(TI,FC	965-635-25	1	2H
17	IC, 6N136 OPTO ISO	965-570-09	2	4S,5S
18	IC, LM393 DUAL COMP(8DIP) (NL)	965-580-00	1	1M
19	MAIN PROGRAM DECODE ADDRESS PROM	231-7053-00	1	3H
20	IC, 4334-3 1KX4 CMOS RAM (HIT)	965-613-13	6	4B-4G
21	IC, AM26LS33 PC QUAD RS422 RCVR	965-640-01	1	2R
22	IC, DS75150J-8	965-642-00	1	1P
23	IC, MC14411 BIT RATE GEN	965-639-00	1	1R
24	IC, XC6850 ACIA (MOT)	965-613-04	1	2L

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, CPU	MODEL NO. 235	231-4340-01	D
		DATE 2-28-80	SHEET 4 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	IC, K1100A OSCILATOR 7.86432MHZ	965-588-00	1	Y2
26	IC, 68B00 2MHZ 6800 CPU	965-613-14	1	4N
27	IC, MC3459 QUAD NAND GATE	965-507-01	1	3P
28	IC, 8T97 HEX BUFFER, TRI ST	965-643-01	3	1D,2N,4A
29	IC, 74LS74	965-635-19	2	1C, 1H
30	IC, 74LS08	965-635-18	1	2D
31	IC, 74LS163	965-635-49	1	5P
32	IC, HCPL2731	965-570-05	1	1B
33				
34	RES, CARBON 1/4W ± 5%, 680	942-206-81	3	R33-R35
35	RES, CARBON 1/2W ± 5%, 100	942-301-01	1	R10
36	RES, FILM RN55C 1% 82	924-308-20	1	R30
37	RES, CARBON 1/4W ± 5%, 100	942-201-01	5	R5,R26,R27 R37,R7
38	RES, CARBON 1/4W ± 5%, 1K	942-201-02	3	R4,R56,R65
39	RES, CARBON 1/4W ± 5%, 10K	942-201-03	2	R60,R61
40	RES, CARBON 1/4W ± 5%, 1M	942-201-05	1	R17
41	RES, CARBON 1/4W ± 5%, 10M	942-201-06	1	R47
42	RES, CARBON 1/4W ± 5%, 27Ω	942-202-70	1	R3
43	RES, CARBON 1/4W ± 5%, 15M	942-201-56	1	R31
44	RES, CARBON 1/4W ± 5%, 20K	942-202-03	5	R20,R22,R28, R29,R43
45	RES, CARBON 1/4W ± 5%, 220	942-202-21	5	R16,R50-R53
46	RES, CARBON 1/4W ± 5%, 330	942-203-31	3	R19,R25,R63
47	RES, CARBON 1/4W ± 5%, 3.3K	942-203-32	7	R40,R46,R54,R55 R57,R58,R6
48	RES, CARBON 1/4W ± 5%, 47K	942-204-73	2	R21,R2

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, CPU	MODEL NO. 235	DATE 2-28-80	SHEET 5 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	RES, CARBON 1/4W ± 5%, 6.8M	942-206-85	1	R45
50	RES, CARBON 1/4W ± 5%, 220K	942-202-24	1	R44
51	RES, CARBON 1/4W ± 5%, 15	942-201-50	2	R12,R13
52	RES, CARBON 1/4W ± 5%, 470	942-204-71	2	R11,R14
53	RES, CARBON 1/4W ± 5%, 270	942-202-71	1	R64
54	RES, CARBON 1/4W ± 5%, 33K	942-203-33	1	R62
55	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	1	R38
56	RES NETWK 1K SIP(785-3-RIK)BEC	952-010-01	2	RN4,RN5
57	RES NETWK, 10K 785-1-R10K	952-010-02	3	RN1,RN2,RN3
58	RES NETWK, 2.2K SIP 785-1-R2.2K	952-022-01	1	RN6
59	RES, CARBON 1/4W ± 5%, 130	942-201-31	1	R24
60	RES, CARBON 1/4W ± 5%, 390	942-203-91	1	R59
61	RES, CARBON 1/4W ± 5%, 2.2K	942-202-22	2	R23,R1
62				
63	POT, 50K BECKMAN (68X)	960-050-02	1	R41
64	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	3	C15,C16,C2
65	CAP, DISC, 100 PF @ 1KV (5GA)	901-011-01	4	C44, C9,C10,C11
66	CAP, TANT, 1 @ 25V(162D)	916-001-25	1	C3
67	CAP,AXIAL .01/50V 180/25V050A	900-021-07	20	C7,8,14,23,26,C1 28,30-35,36-42
68	CAP, TANT, 10 @ 10V (162D)	916-010-10	2	C27,C29
69	CAP,.1MF@50V(VARADYNE 1802)	900-021-08	1	C12
70	CAP, .01MF/50V(3429-050E-1032)	900-021-01	8	C17-C22, C25 C24,
71	CAP, DISC. .01 @ 500V	900-021-04	1	C43
72	CAP, TANT,1 @ 50V (196D)	916-010-05	2	C6, C13

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, CPU	MODEL NO. 235	231-4340-01	D
		DATE 2-28-80	SHEET 6 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74				
75	DIODE, ZENER 1N5226 5.1V	961-522-60	2	CR5,CR6
76	DIODE, 1N914 (1N4148)(TD,FC,TI	961-091-40	12	CR1-CR3,CR7, CR12-CR-19
77	DIODE, ZENER 1N5221 B	961-522-12	1	CR4
78				
79				
80				
81				
82	65K ROM1 V18 8000-9FFF	231-7010-00	1	4I
83	65K ROM2 V18 A000-BFFF	231-7020-00	1	4J
84	65K ROM3 V18 C000-DFFF	231-7030-00	1	4K
85	65K ROM4 V18 E000-FFFF	231-7040-00	1	4L
86				
87				
88				
89				
90				
91	RECTIFIER, BRIDGE, WL005M (GI)	966-002-26	2	CR10,CR11
92	IC SOCKET, 24 1P(AG) 524-AG37D	992-010-35	2	4H,3H
93				
94	IC SOCKET, 40DIP (540-AG37D	992-010-36	1	4N
95	CONN, RECEPT 25PIN(AMP745-106-2)	973-010-75	1	J2
96	SWITCH,DIP-6P1T(SEALED GH76SB06S)	969-050-13	1	S3

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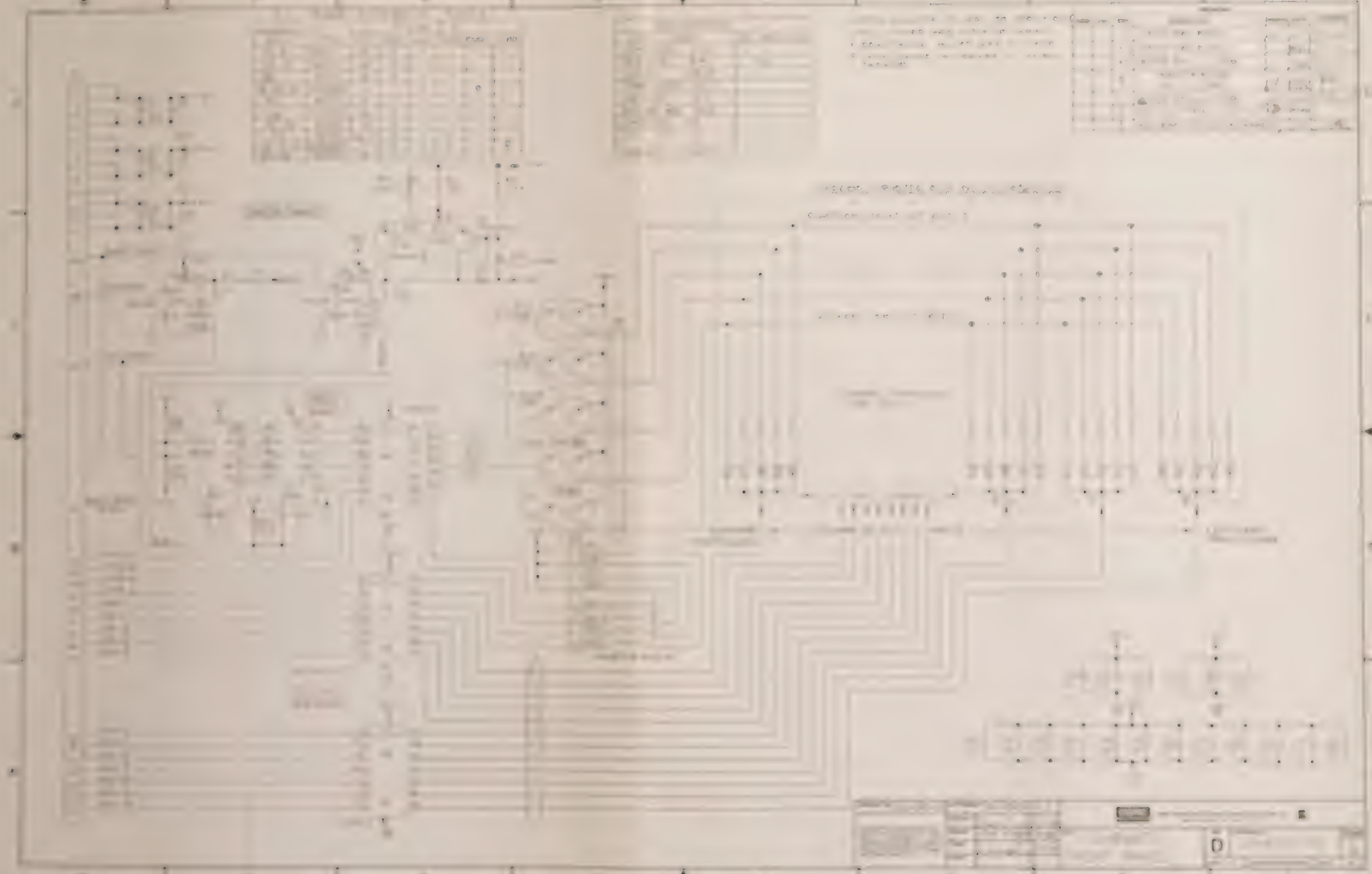
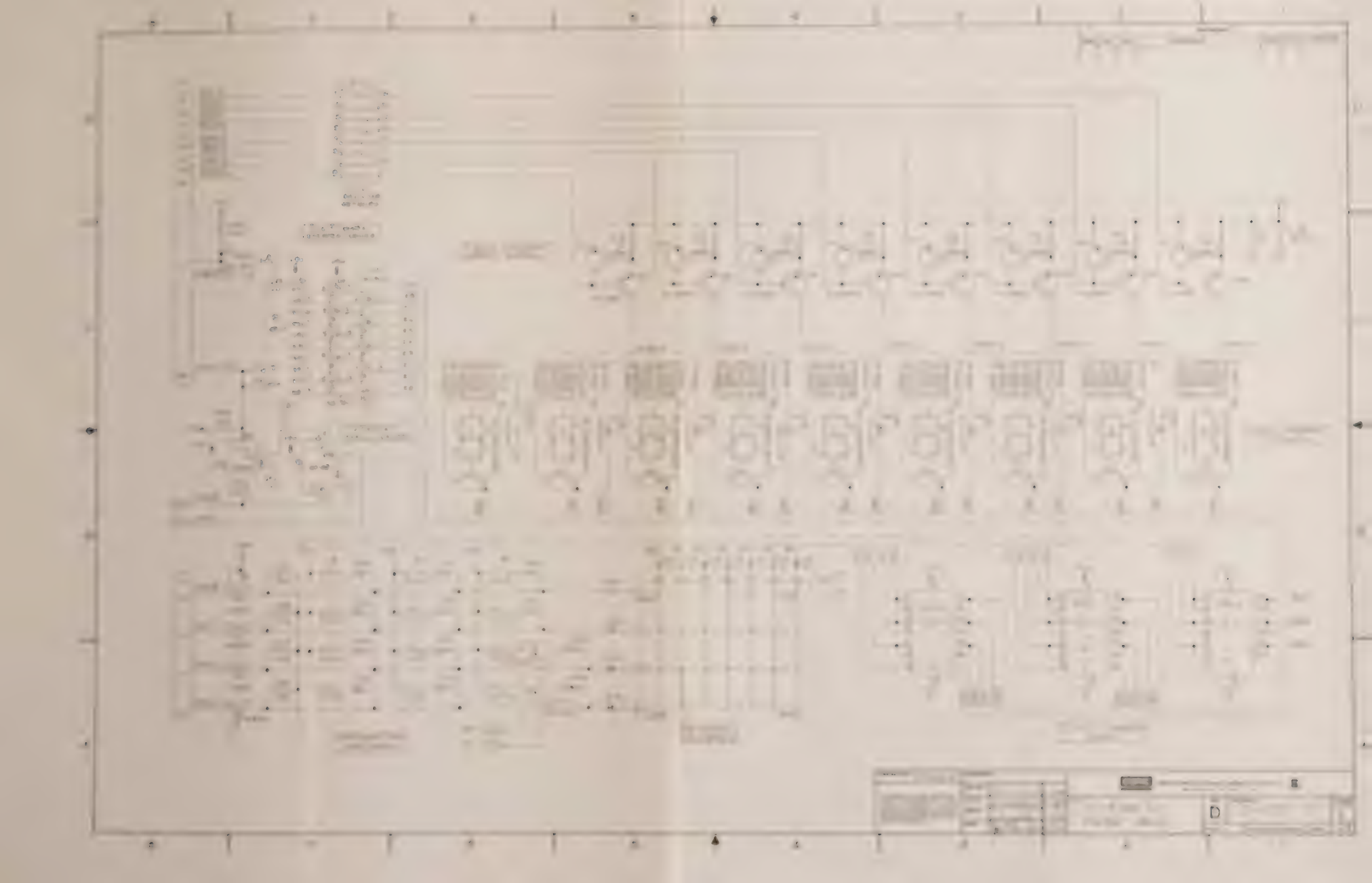
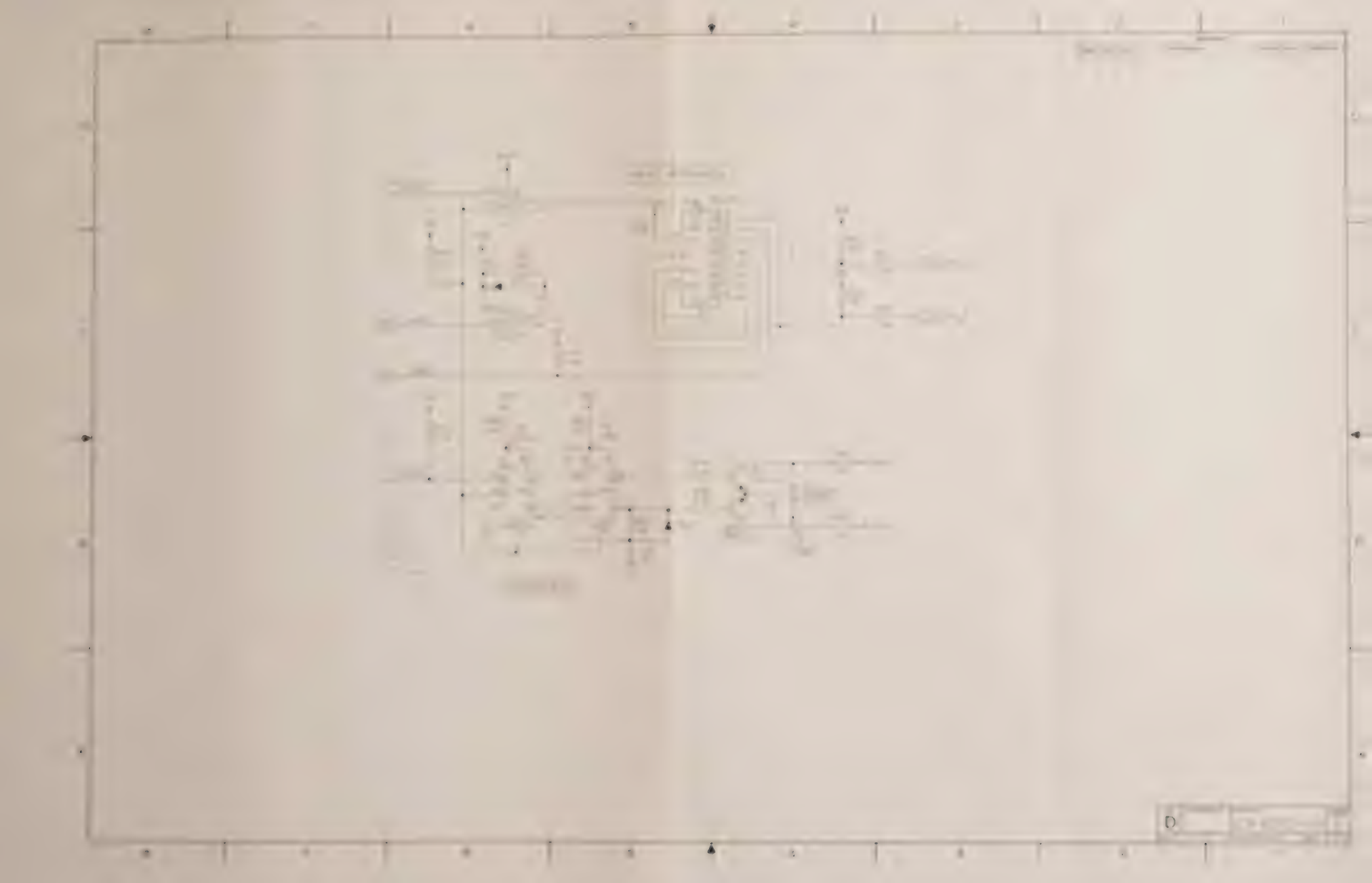
MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, CPU	MODEL NO. 235	231-4340-01	D
		DATE 2-28-80	SHEET 7 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
97	SWITCH, DIP3POS 1PDT GH(76TCO	969-050-09	1	S4
98	XSTR, MPSA13 (NPNA/DR192)(M)	964-040-03	3	Q2,Q8,Q1
99	XSTR, pN3646 (NPNSH106)(MO,FC)	962-364-60	3	Q9,Q10,Q11
100	XSTR, pN4250 (PNPA)(FC,NL)	962-425-00	4	Q4,Q5,Q6,Q7
101	XSTR, PN2222 (NPNA92)(NA)	962-222-20	1	Q12
102	ICL8069 REFERENCE 1.22V	961-501-02	1	CR9
103	XTAL, 1,8432 MHZ HC-33	967-005-16	1	Y1
104	XSTR, PN3640	962-364-00	1	Q3
105	SWITCH, DPDT 76SD02S (GRAYHILL)	969-050- 15	1	S2
106				
107	CONN, RECPT 9PIN(AMP745102-2)	973-010-77	1	J1
108	SWITCH, ALCO TPA11FG-PC-2	969-050-16	1	S1
109	SCREW,PAN HD. PHILLIPS 4-40 X 3/8	980-440-038	4	J1,J2
110	NUT, HEX RADIAL 4-40	984-200-440	4	J1,J2
111	BATT 2.4V GE 41B901BD11G1	975-100-08	1	INSTALL AT BT1 TEST LEVEL
112	CHASSIS FSNR 632B2 (US1590B1)	991-020-26	1	
113	WASHER SPLIT LOCK NO. 4	986-200-04	4	J1,J2
114	WASHER FLAT NO. 4	986-100-04	4	J1,J2
115	SCREW PHMS 6-32 X 1/2 LG	980-632-050	1	
116	WASHER FLAT NO. 6	986-100-06	1	
117	WASHER SPLITLOCK NO. 6	986-200-06	1	
118				
119				
120				







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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, FRONT PANEL BOARD	MODEL NO. 235	DATE	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, FRONT PANEL BOARD	231-2320-00	1	
2	SCHEMATIC	231-6320-00	1	
3	TEST SPEC			
4				
5				
6	IC, 4001 4-2IN NOR CMOS	965-587-01	1	4B
7	IC, 4017 COUNTER/DIV CMOS (MO)	965-587-18	2	2C,4C
8	IC, 74C221 DUAL MONO(FC,NL,MO)	965-587-45	2	1E,4A
9	IC, 4040 12BIT BIN CTR	965-587-46	2	3C,3D
10	IC, 4503 TRI-STATE HEX BUFFER	965-587-69	1	4D
11	IC, 74C907 OPEN D PMOS HEX BUF	965-587-71	2	2B,2D
12	IC, 4010 CMOS BUFFER	965-587-73E	1	2A
13	IC, ULN2003A,7DARL ARRAY(SPFMO)	965-625-01	6	1B,1C,1D,2E,3E, 4E
14	IC, 74LS175 QUAD D F/F	965-635-46	1	3B
15				
16				
17				
18				
19				
20	RES, CARBON 1/4W ± 5%, 10	942-201-00	8	R16-R23
21	RES, CARBON 1/4W ± 5%, 1K	942-201-02	1	R45
22	RES, CARBON 1/4W ± 5%, 10K	942-201-03	14	R31-R35,R37,R39 R43,R27-30,R46,R6
23	RES, CARBON 1/4W ± 5%, 20K	942-202-03	5	R11-R15
24	RES, CARBON 1/4W ± 5%, 2.2K	942-202-22	3	R7, R41,R42

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, FRONT PANEL BOARD	MODEL NO. 235	231-4320-00.	D
	DATE	SHEET 4 OF 5	

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25				
26				
27	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	5	R8,R9,R10,R47 R38
28	RES, CARBON 1/4W ± 5%, 47K	942-204-73	3	R25,R26,R1
29	RES, CARBON 1/4W ± 5%, 620	942-206-21	1	R24
30	RES, CARBON 1/4W ± 5%, 820	942-208-21	1	R3
31	RES NWK, 2.2K 16 DIP (898-3-R2.2K)	951-022-01	1	RN1
32				
33	RES, CARBON 1/4W ± 5%, 330	942-203-31	1	R40
34	RES, CARBON 1/4W ± 5%, 100K	942-201-04	1	R36
35				
36				
37	CAP, .1MF@50V(3429-050E-104Z)A	900-021-02	1	C1
38	CAP, .01/50V 1801Z5U050A	900-021-07	24	C7,C9,C11,C13-C31,C32,C3
39	CAP, 1UF @ 50V (196D)	916-010-05	2	C5,C2
40	CAP, 10MF @ 10V (162D)	916-010-10	4	C4,C8,C10,C12
41	CAP, 22UF @ 35V (196D)	916-220-05	1	C6
42				
43				
44				
45				
46				
47	DIODE, 1N702 (3.2V) (TD,MO)	961-070-20	1	CR2
48	DIODE, 1N914 (1N4148)(TD,FC,TI	961-091-40	26	CR1,CR3-CR27

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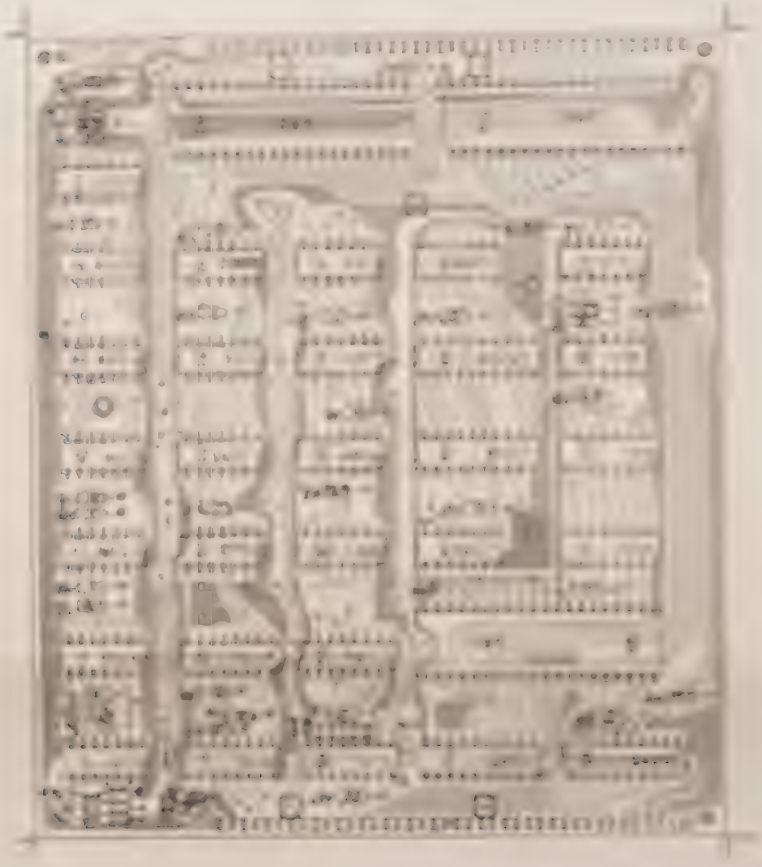
MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY PCB, FRONT PANEL BOARD	MODEL NO. 235	DATE 4-15-80	SHEET 5 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49				
50				
51				
52				
53				
54	THERMISTER 100 K JT51J5(FENWAL)	955-001-04	1	R5
55	POT, 10K CERMET 72PL	960-101-03	1	R44
56				
57	POT, 5K CERMET 72PL	960-100-53	1	R4
58	XSTR, PN2222 (NPNA92) (NA)	962-222-20	2	Q21,Q22
59	XSTR, PN2907 (PNP) (NSC)	962-290-70	18	Q3-Q20
60	XSTR, 2N4250 (PNPA) (FC,NL)	962-425-00	2	Q1,Q2
61	XSTR, MJE700, (PNPA77)(NA,MO)	964-047-00	5	Q23-Q27
62	LED, RED (MV5753)	968-010-11	8	DS10-DS17
63	DISPLAY, 1 DIGIT LED, MAN 6680	968-084-01	9	DS1-DS9
64	SWITCH DIP-4P SEALED(GH76SB04S)	969-050-12	3	S1,S2,S3
65	CONN, 17PC/FC HBLB17S3 BURNDY	973-010-48	1	J4
66	CONN PC 50 RIBBON (3M3433-2203)	973-060-10	1	P1
67	TERM STICK 8M (65610-108) BERG	973-381-00	1	P3
68	CONN, 12 PIN MOLEX 15-25-4121	973-370-11	1	J2
69	XDUCER, CERAMIC SK-173	994-001-00	1	Y1
70	SOLID 24 AWG, TEFLON INS WIRE	978-300-00	2"	Y1
71				
72				



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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, PIA BOARD	MODEL NO. 235	231-4310-00	F
		DATE 4-15-79	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, PIA BOARD	231-2310-03	1	
2	SCHEMATIC	231-6310-00	1	
3	TEST SPEC		1	
4				
5				
6	IC, 4011 4-2IN NAND CMOS(MO)	965-587-02	1	3C
7	IC, 74C04(4069)HEX INV CMOS(RC)	965-587-05	1	3D
8	IC, 4024 7-ST BIN CNTR CMOS(FC)	965-587-22	1	1B
9	IC, 4013 DUAL D FF CMOS(FC,MO)	965-587-23	1	1A
10	IC, 4070 4-EXCL OR CMOS (FC)	965-565-05	1	5E
11	IC, 4021 8STG SR(FC,NL,MO)	965-587-43	2	5C,5D
12	IC, 6821 PIA (MO,FC)	965-613-10	3	2H,4B,3H
13	IC, 74LS04 HEX INV(FC,MO,NL)	965-635-00	2	1E,2C
14	IC, 74LS245 8 BUS XCVR(TI,FC)	965-635-04	2	4A,5A
15	IC, 74LS374J 8 3-ST REG(AMD,F)	965-635-05	2	4D,4E
16	IC, 74LS393 DUAL 4BIN CTR(FC,TI	965-635-06	3	2D,4C,4F
17	IC, 74LS00 4-2IN NAND (TI)	965-635-07	1	3E
18	IC, 74LS10 3-3IN NAND (TI)	965-635-08	1	3F
19	IC, 74LS02 QUAD 2 IN NOR	965-635-17	1	2F
20	IC, 74LS74 DUAL D F/F	965-635-19	5	1C,1D,1F,2E,5F
21	IC,74LS20 DUAL 4-IN POSNAND	965-635-35	1	1H
22	IC, 74LS156	965-635-48	1	3B
23				
24				

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, PIA BOARD	MODEL NO. 235	231-4310-00	F
		DATE 4-[illegible]-80	SHEET 4 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25				
26				
27				
28				
29	RES, CARBON 1/4W ±5%, 2.2K	942-202-22	1	R16
30				
31	RES, CARBON 1/4W ± 5%, 1K	942-201-02	10	R9-10,R13-15, R17-18,R20-22 R19
32	RES, CARBON 1/4W ± 5%, 10K	942-201-03	5	R4,R7,R24,R23
33	RES, CARBON 1/4W ± 5%, 20K	942-202-03	1	R12
34	RES, CARBON 1/4W ± 5%, 6.8K	942-206-82	7	R1,R2,R5,R8,R11 R3,R25
35	RES NTWK 6.8K SIP(785-1-R6.8K)	950-068-01	1	RN1
36	RES, CARBON 1/4W ± 5%, 51Ω	942-205-10	1	R6
37	RES NTWK 4.7K SIP(783-1-R4.7K)	953-047-01	1	RN2
38				
39				
40				
41				
42	CAP,AXIAL .01/50V 180/Z5V050A	900-021-07	16	C2,C4-16,C18, C19
43	CAP, MICA, .001	915-031-02	1	C1
44	CAP, 10uf, TANT 10V (162D)	916-010-10	3	C3,C17,C20
45				
46				
47				
48				

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, PIA BOARD	MODEL NO. 235	231-4310-00	F
		DATE 4-15-80	SHEET 5 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49				
50	SELEC TED 4051 CMOS MULTI	000-8050-00	3	2A,2B,3A
51	XSTR, 2N3640 (PNP)(FC,NL)	962-364-00	1	Q1
52	CONN, PC20M (MOLEX 22-10-2201)	973-010-112	4	P1,P2

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY PCB, POWER SUPPLY	MODEL NO. 235	DATE 4-15-80	SHEET 4 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, POWER SUPPLY	231-2500-03	1	
2	SCHEMATIC	231-6500-00	1	
3	TEST SPEC		1	
4				
5				
6				
7	IC, LM393 DUAL COMP(8DIP)(NL)	965-580-00	1	Z1
8	IC, 4049 HEX INV CMOS (FC,MO)	965-587-21	1	Z3
9	IC, 4013 DUAL D FF CMOS (FC,MO)	965-587-23	1	Z4
10	IC, LM3086 5 XSTR ARRAY (NL)	965-631-00	1	Z2
11	IC, -12V REG., LM320LZ-12 (NL)	965-551-03	1	Z5
12	IC, +12V REG., LM78L12ACZ (NL)	965-551-04	1	Z6
13				
14				
15				
16	RES, FILM RN60C, 1.0K	920-410-01	1	R8
17	RES, FILM RN60C, 2.61K	920-426-11	1	R6
18	RES, CARBON 1/4W ± 5%, 10	942-201-00	2	R52,R39
19	RES, CARBON 1/4W ± 5%, 100	942-201-01	2	R47,R37
20	RES, CARBON 1/4W ± 5%, 1K	942-201-02	3	R49,R25,R23,
21	RES, CARBON 1/4W ± 5%, 10K	942-201-03	4	R26,R27,R28,R2
22	RES, CARBON 1/4W ± 5%, 100K	942-201-04	4	R16,R15,R19,R3
23	RES, CARBON 1/4W ± 5%, 1M	942-201-05	4	R20,R18,R17,R13
24	RES, CARBON 1/4W ± 5%, 120K	942-201-24	1	R9

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO	REV
ASSEMBLY PCB, POWER SUPPLY	MODEL NO. 235	231-4500-02	H
		DATE	SHEET 5 OF 9

ITEM NO	DRAWING TITLE	DRAWING NO	NO. REQ	REMARKS
25	RES, CARBON 1/4W ± 5%, 150	942-201-51	1	R1
26	RES, CARBON 1/4W ± 5%, 15K	942-201-53	3	R22,R21,R24
27	RES, CARBON 1/4W ± 5%, 2.2K	942-202-22	1	R48
28	RES, CARBON 1/4W ± 5%, 220K	942-202-24	2	R12,R38
29	RES, CARBON 1/4W ± 5%, 33	942-203-30	4	R29-R32
30	RES, CARBON 1/4W ± 5%, 330	942-203-31	1	R4
31	RES, CARBON 1/4W ± 5%, 47	942-204-70	1	R51
32	RES, CARBON 1/4W ± 5%, 470	942-204-71	2	R35,R36
33	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	2	R14,R5
34	RES, CARBON 1/4W ± 5%, 470K	942-204-74	2	R44,R43
35	RES, CARBON 1/4W ± 5%, 56K	942-205-63	1	R34
36	RES, CARBON 1/2W ± 5%, 1	942-301-00	1	R54
37	RES, CARBON 1/2W ± 5%, 2.2K	942-302-22	1	R50
38	RES, CARBON 1/2W ± 5%, 3.0	942-303-09	1	R53
39	RES, CARBON 1/2W ± 5%, 330K	942-303-34	1	R45
40	RES, CARBON 1/2W ± 5%, 470K	942-304-74	1	R46
41	RES, CARBON 5W ± 5%, 2	942-602-00	2	R42,R41
42	RES NETWORK 15K SIP 764-3-R15K	950-015-02	1	RN1
43	RES, CARBON 1/4W ± 5%, 8.2K	942-208-22	2	R11,R55
44	RES, CARBON 1/4W ± 5%, 3.3K	942-203-32	1	R40
45	RES, CARBON 1/2W ± 5%, 1K	942-301-02	1	R33
46				
47				
48	CAP, .1MF@50V(3429-050E-104Z)A	900-021-02	1	C12

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY PCB, POWER SUPPLY	MODEL NO. 235	231- 4500-02	H
		DATE 4-15-80	SHEET 6 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	CAP, DISC, .01 @ 500V (5GA)	900-021-04	3	C28,C3,C1
50	CAP, DISC,.001 @ 1KV (5GA)	900-081-03	2	C29,C2
51	CAP, .1 @ 50V, VARADYNE 1802Z5U	900-021-08	2	C20,C23
52	CAP, DISC, 100 PF @ 1KV (5GA)	901-011-01	3	C8,C9,C30
53	CAP, ELT, 100/20V SPRG 672D-CG5	910-100-20	1	C21
54	CAP, ELT 180/12V SPRG 672D-CG5	910-180-12	1	C15
55	CAP, ELCTLT, 85@ 150V (39D)	910-851-50	1	C7
56	CAP, ELCTLT 90/200V (39D)	910-902-00	2	C27,C26
57	CAP, ELCTLT 1000/6.3V	910-100-06	1	C17
58	CAP, DISC, .01MF @ 1KV	900-021-05	1	C32
59	CAP, MICA 1200 PF (CD15-FA122GO3)	915-031-22	1	C6
60	CAP, TANT 2.2 @ 35V(196D)	916-220-04	1	C13
61	CAP,.001 @ 50V, VARADYNE 1801X7R	900-021-09	1	C5
62	CAP, SF, .1/100V,SMS(B32570)	918-001-10	3	C11,C10,C4
63	CAP, .1 250V SF SIEMENS (B32570)	918-001-25	1	C14
64	CAP, 1 100V SF SIEMENS(B32571)	918-010-10	3	C16,C22,C19
65	CAP, MYLAR, .1 @ 400V (ZA2E)	912-010-40	1	C18
66	CAP, DISC, 470pF @ 1KV (5GA)	901-014-71	1	C31
67	CAP, TANT 3.3 @ 25V (1620)	916-033-25	1	C33
68				
69				
70	DIODE, 1N457A (LOLEAK)(TD,FC)	961-045-70	2	CR6,CR7
71	DIODE, 1N759 (12V) (TD,MO)	961-075-90	1	CR5
72	DIODE, 1N914 (1N4148)(TD,FC,TI)	961-091-40	17	CR2,4,9,11-13, 15,18-21,37-40

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY PCB, POWER SUPPLY	MODEL NO. 235	231-4500-02	H
		DATE 4-15-80	SHEET 7 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73	DIODE, 1N4933(1A/50V,FAST)(MO)	961-493-30	4	CR27-30
74	DIODE, 1N4937(1A/600V,FAST) MO	961-493-70	5	CR14,16,41,44,45
75	DIODE, 8069 DCQ INTERSIL	961-501-02	1	CR1
76	DIODE, 1N5229B 4.3V (MO)	961-522-92	1	CR3
77	DIODE, 1N5232 B 5.6V	961-523-22	2	CR17,CR26
78	DIODE, 1N5270B 91V	961-527-02	2	CR8,CR36
79				
80				
81				
82				
83	POT 5K CERMET (72XL)	960-015-11	1	R10
84	TRANSFORMER, INVERTER	231-7000-00	1	T1
85	TRANSFORMER, SWITCHING	230-7020-01	1	T3
86	TRANSFORMER, PULSE	230-7022-00	1	T2
87	POT, 1K CERMET (72XL)	960-011-25	1	R7
88	XSTR PN2222 (NPN) (NA)	962-222-20	3	Q13,Q14,Q15
89	XSTR, PN2907 (PNP) (NSC)	962-290-70	1	Q1
90	XSTR, 2N4250 (PNP) (FC,NL)	962-425-00	1	Q2
91	SCR, 2N4441 (8A PLASTIC)(MO)	962-444-10	1	Q12
92	XSTR, 92PU01A(NL)	964-040-01	2	Q5,Q7
93	XSTR, 92PU10(NL)	964-040-10	2	Q4,Q9
94	XSTR, 92PU51A (NL)	964-040-51	2	Q6,Q8
95	XSTR, MPSA92 (PNPA) (MO)	964-040-92	1	Q3
96	XSTR, MJE13005	964-130-05	3	Q10,Q11,Q16

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, POWER SUPPLY	MODEL NO. 235	231-4500-02	H
		DATE 4-15-80	SHEET 8 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
97	OPTO FCD 825B (FC)	965-570-08	1	OC2
98	RECTIFIER, 1N4005 600V 1A(DI)	966-002-04	6	CR10,CR31-35
99	RECTIFIER, FAST 3AMP 50V	966-002-08	4	CR22-25
100	CHOKE, 50 MICROHENRY	967-005-14	2	L1,L3
101	HP5082-4350 6N135 OPTO ISO	965-570-00	1	OC1
102	SVP, 270V SMS B2-B270	967-006-01	1	SG2
103	SVP, 470V SMS B2-B470	967-006-02	1	SG1
104	WFR ASSY, 7CKT(09-75-1071)MOLEX	973-070-12	1	P2
105	WFR ASSY, 6CKT(09-75-1061)MOLEX	973-070-11	1	P3
106	HEAT SINK, THERMALLY THM6073	991-008-00	3	HS1-HS3
107	WFR ASSY, 2CKT(09-75-1021)MOLEX	973-070-25	1	P4
108	INDUCTOR, 5.6UH, CAMBION	967-005-02	1	L2
109	SHIELD, POWER SUPPLY	231-2630-00	1	
110	CHASSIS FSNR 632B2(US1590B1)	991-020-26	1	
111	SCREW, PAN HD PHILLIPS, 4-40 X 3/8	980-440-038	4	
112	SCREW, NYLON PAN HD SLOT 6-32 X 15/16	983-632-0937	1	
113	SCREW, NYLON PAN HD SLOT 4-40 X 1/2	983-440-050	1	
114	SCREW, PAN HD PHILLIPS, 6-32 X 5/16	980-632-031	3	
115	HEX NUT 4-40	984-100-440	1	
116	HEX NUT 6-32	984-100-632	1	
117	HEX NUT, RADIAL 6-32	984-200-632	3	
118	WASHER, SPLITLOCK 4	986-200-04	4	
119	WASHER, SPLITLOCK 6	986-200-06	3	
120	WASHER, FLAT NYLON 4	986-800-00	1	

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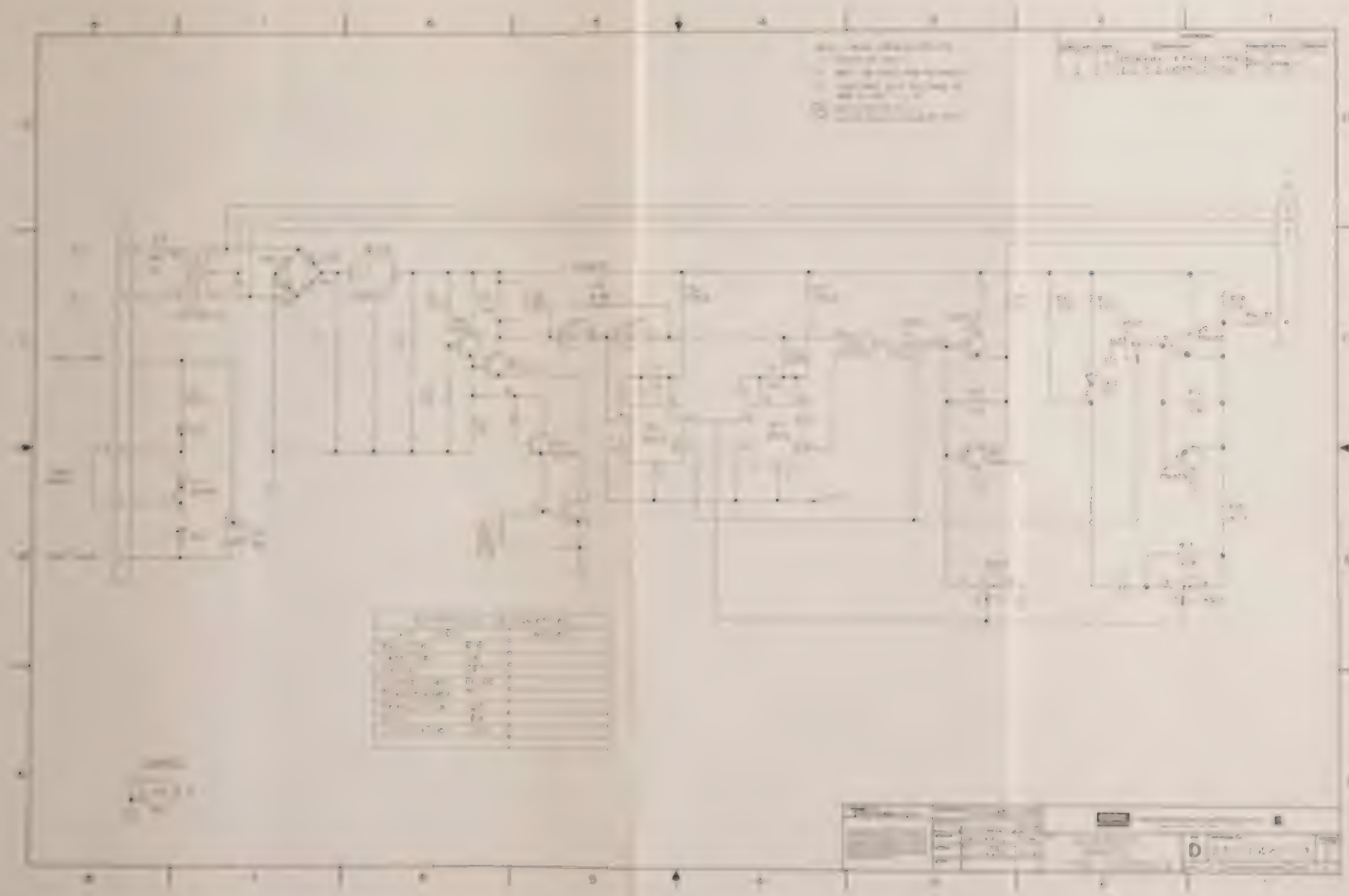
MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, POWER SUPPLY	MODEL NO. 235	231-4500-02	H
		DATE 8-20-80	SHEET 9 OF 9

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
121	WASHER, FLAT NYLON 6	986-800-04	1	
122	WASHER, INT STAR 4	986-400-04	1	
123	WASHER, INT STAR 6	986-400-06	1	
124	LABEL, HI-VOLTAGE (T&B#WCSS76F)	991-060-10	1	
125	JUMPER, J.500X.125T22	991-010-05	3	JMP 1 - JMP 3



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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSY PCB, REMOTE FEM INTERFACE	MODEL NO. 230A 235	DATE 6-25-80	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, REMOTE FEM INTERFACE	230-2480-03	1	
2	SCHEMATIC	230-6480-03	1	
3	TEST SPEC		1	
4				
5				
6	IC, 4011 4-2IN NAND CMOS (MO)	965-587-02	1	Z2
7	IC, 4528 MONO-VIB CMOS (FC,MO)	965-587-14	1	Z3
8	IC, 4503 TRI-STATE HEX BUFFER	965-587-69	1	Z4
9	IC, LM78L08 ACZ	965-637-01	1	Z1
10				
11				
12				
13				
14				
15	RES, 1/4W ±5%, 330	942-203-31	1	R11
16	RES, 1/4W ±5%, 10K	942-201-03	5	R3,R8,R10,R12, R14
17	RES, 1/4W ±5%, 20K	942-202-03	2	R2,R13
18	RES, 1/4W ±5%, 220	942-202-21	1	R1
19	RES, 1/4W ±5%, 33	942-203-30	2	R9,R16
20	RES, 1/4W ±5%, 330K	942-203-34	2	R6,R1
21	RES, 1/4W ±5%, 4.7K	942-204-72	1	R15
22	RES, 1/4W ±5%, 6.8K	942-206-82	1	R5
23	RES, 1/4W ±5%, 1.3K	941-201-32	1	R4
24	RES, 1/4W ±5%, 680	942-206-81	1	R17

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSY PCB, REMOTE FEM INTERFACE	MODEL NO. 230A 235	DATE 6-25-80	SHEET 4 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25				
26				
27				
28				
29				
30	CAP, .1MF@50V(3429-050E-104Z)	900-021-02	2	C1,C7
31	CAP, AXIAL .01/50V 180/25V050A	900-021-07	2	C2,C3
32	CAP, DISC. .001@ 1KV (5GA)	900-081-03	2	C4,C5
33	CAP, DISC. 100 PF @ 1KV (5GA)	901-011-01	1	C6
34	CAP, DISC. 470 PF @ 1KV (5GA)	901-014-71	1	C8
35				
36				
37				
38				
39	DIODE, 1N914 (1N4148) (TD,FC,T1)	961-091-40	6	CR1-CR6
40				
41				
42				
43				
44				
45	XFMR, REMOTE FEM INTER	230-7080-01	1	T1
46	THERMISTOR RL5506-5-120-30PT2	955-000-05	1	R18
47	XSTR, PN2222 (NPNA92)(NA)	962-222-20	4	Q1,Q2,Q3,Q5
48	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	2	Q4,Q6

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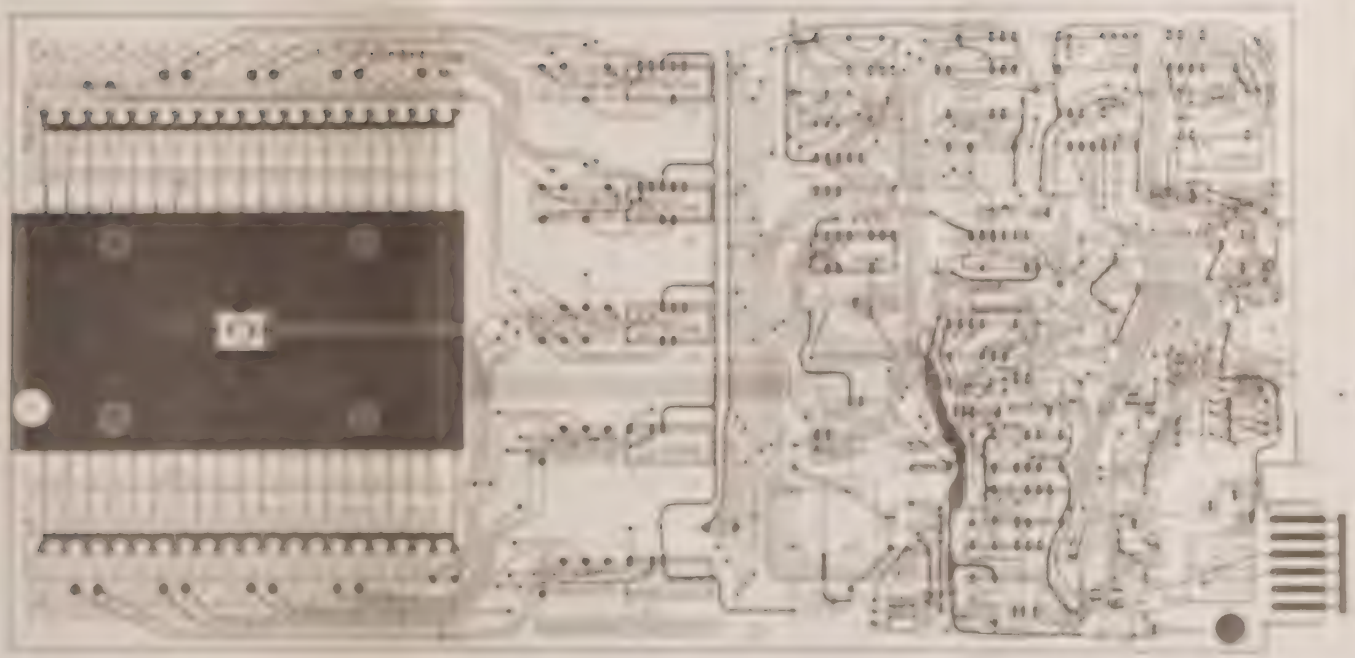
MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSY PCB, REMOTE FEM INTERFACE	MODEL NO. 230A 235	230-4480-03	D
		DATE 6-25-80	SHEET 5 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	OPTO, FCD831B (FC)	965-570-03	1	OC2
50	CHASSIS FSTNR, 632B2 (US1590B1)	991-020-26	2	
51	OPTO 6N138	965-570-01	1	OC1
	THE FOLLOWING PARS ARE TO BE ADDED IN TEST:			
51	REAR PANEL REMOTE FEM INT	230-2890-00	1	
52	SCREW MAC. 6-32 X 3/8: PHMS	980-632-038	2	
53	WASHER FLAT #6	986-100-06	2	
54	WASHER SPLITLOCK #6	986-200-06	2	



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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY SOLID STATE FEM	MODEL NO. 235	230-4400-02	S
		DATE 3-18-80	SHEET 3 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB SOLID STATE FEM	230-2400-02	1	
2	SCHEMATIC	231-6400-02	1	
3	TEST SPEC		1	
4				
5				
6	IC, LM393 DUAL COM(8DIP)(NL)	965-580-00	1	Z24
7	IC, 4001 4-2IN NOR CMOS (MO)	965-587-01	1	Z15
8	IC, 4015 DUAL SR CMOS (MO)	965-587-03	1	Z8
9	IC, GRADED 4066	000-8130-00	1	Z13
10	IC, 4013 DUAL D FF CMOS (FC,MO)	965-587-23	1	Z10
11	IC, 74C42 BCD-DECIMAL DEC CMOS	965-587-34	1	Z6
12	IC, 4040 12BIT BIN CTR(MO,FC)	965-587-46	1	Z9
13	IC, 4555 DUAL 10F4 NI(MO,FC,NL	965-587-68	1	Z14
14	IC, 301A OPAMP(8DIP)(NL,SG)	965-592-01	1	Z19
15	IC, LF351N FET OP AMP(NL)	965-616-01	2	Z20,Z21
16	IC, 4572 INV,NOR,NAND CMOS (MO)	965-618-00	2	Z16,Z25
17	IC, LM329BZ 20PPM REF (NL)	965-636-00	1	Z23
18	IC, LM78L15ACZ 15V REG92(NL)	965-637-00	1	Z22
19				
20				
21				
22				
23				
24	RES, FILM RN60C 1% 499K	920-449-93	1	R79

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY SOLID STATE FEM	MODEL NO. 235	230-4400-02	S
		DATE 3-18-80	SHEET 4 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN55D 1% 10K	924-310-02	1	R56
26	RES, FILM RN55C 1% 2K	924-420-01	2	R53,R54
27	RES, FILM RN55C 1% 6.98K	924-469-81	1	R44
28	RES, FLAMEPROOF 1/4W ±5%, 10	940-001-00	1	R91
29	RES, CARBON 1/4W ± 5%, 100	942-201-01	2	R58,R59
30	RES, CARBON 1/4W ± 5%, 1K	942-201-02	2	R41,R42
31	RES, CARBON 1/4W ± 5%, 10K	942-201-03	2	R60,R68
32	RES, CARBON 1/4W ± 5%, 100K	942-201-04	5	R62,73,84,87 & 89
33	RES, CARBON 1/4W ± 5%, 150	942-201-51	2	R52,R82
34	RES, CARBON 1/4W ± 5%, 15K	942-201-53	1	R88
35	RES, CARBON 1/4W ± 5%, 10M	942-201-06	1	R92
36	RES, CARBON 1/4W ± 5%, 20K	942-202-03	9	R45-46,R49-51,57 R66-67,R74
37	RES, CARBON 1/4W ± 5%, 220	942-202-21	2	R69,R80
38	RES, CARBON 1/4W ± 5%, 220K	942-202-24	2	R81,R83
39	RES, CARBON 1/4W ± 5%, 33K	942-203-33	1	R90
40	RES, CARBON 1/4W ± 5%, 3.9K	942-203-92	1	R48
41	RES, CARBON 1/4W ± 5%, 39K	942-203-93	3	R47,R71,R72
42	RES, CARBON 1/4W ± 5%, 470	942-204-71	1	R70
43	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	1	R94
44	RES, CARBON 1/4W ± 5%, 47K	942-204-73	2	R85,R86
45	RES, CARBON 1/4W ± 5%, 680	942-206-81	1	R61
46	RES, CARBON 1/2W ± 5%, 2.2K	942-302-22	40	R1-R40
47				
48				

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, SOLID STATE FEM	MODEL NO. 235	230-4400-02	S
		DATE 3-18-80	SHEET 5 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49				
50				
51	CAP, TANT. 4.7 @ 35V (1960)	916-470-35	1	C71
52	CAP, DISC .01/500V (5GA)	900-021-04	48	C1-40,C61,C65,67 C70, ,73-75,84
53	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	2	C76,C78
54	CAP, DISC, 100 PF @ 1KV (5GA)	901-011-01	5	C62,63,77,83,85
55	CAP,PLP,/.1/200V,IMB(GA2C104K)	917-001-20	1	C79
56	CAP,PLP,.22/200V,IMB(GA2C224K)	917-022-20	1	C82
57	CAP,PLP,.47/200V,IMB(GA2C474K)	917-047-20	2	C66,68
58	CAP, SF, .1/100V, SMS(B32570)	918-001-10	3	C69,72,81
59	CAP, SF, .0022/250V, SMS(32570)	918-002-25	1	C64
60	CAP, SF, .22/100V, SMS(B32570)	918-022-10	21	C41-60,C80
61				
62				
63				
64				
65				
66	DIODE, 1N914 (1N4148)(TD,FC,TI	961-091-40	9	CR4-12
67	DIODE, 1N5229B 4.3V (MO)	961-522-92	1	CR3
68	DIODE, 1N5236B (7.5V)	961-523-62	1	CR2
69				
70	DIODE, 1N5240, 10V	961-524-00	1	CR1
71				
72				

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, SOLID STATE FEM	MODEL NO. 235	DATE 3-18-80	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74				
75				
76	GRADED 4016	000-7700-00	4	Z11,Z12,Z17,Z18
77	SELECTED 4051 CMOS MULTI	000-8050-00	1	Z7
78	SELECTED 4052 CMOS MULTI	000-8051-00	5	Z1-5
79	FET, 2202 (NJ,LO-LK,GP)	100-722-02	3	Q2,Q14,Q15
80	TRANSISTOR(SELECTED-COLOR DOT)	220-7200-01	1	Q1
81	TRANSFORMER, INTERFACE	230-7030-00	1	T1
82	RESISTOR NETWORK, FEM	230-7100-00	1	RN1
83	POT, 1K VISHAY (1280)	960-011-30	1	R63
84	POT, 100 CERMET (72PL)	960-015-19	1	R55
85	POT, 25K MT2X253	960-015-15	2	R43,R93
86	XSTR. PN2222 (NPNA92)(NA)	962-222-20	3	Q8,Q9,Q11
87	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	5	Q3,Q4,Q7,Q10, Q13
88	FET, NPD5566(NJ,LO,NSE,8BIT)NL	962-556-60	1	Q5
89	XSTR, MPSA13 (NPNA/DRL92) (M)	964-040-03	2	Q6,Q12
90	OPTO, FCD831B (FC)	965-570-03	2	OC1,OC2
91	T.S 20P ELCTVT 8145 251352053	973-010-55	2	
92	SPACER, 1/8X6A2(L6310-2-2A)	991-020-88	2	
93	IC SOCKET, 16DIP PC (316AG5DR)	992-010-22	6	
94	DISS-O-PAD .250 O.D. X .125 I.D. X .03 Bivar Inc. TO-16-03	979-020-11	6	

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, REED FEM	MODEL NO. 235	230-4410-03	E
		DATE 3-17-80	SHEET 3 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB REED FEM	230-2410-02	1	
2	SCHEMATIC	231-6410-03	1	
3	TEST SPEC		1	
4				
5				
6	IC, LM393 DUAL COMP(8DIP)(NL)	965-580-00	1	Z4
7	IC, 4001 4-2IN NOR CMOS(MO)	965-587-01	1	Z17
8	IC, 4015 DUAL SR CMOS (MO)	965-587-03	1	Z7
9	IC, GRADED 4066	000-8130-00	1	Z13
10	IC, 4013 DUAL D FF CMOS(FC,MO)	965-587-23	1	Z8
11	IC, 74C42 BCD-DECIMAL DEC CMOS	965-587-34	2	Z2,Z5
12	IC, 4040 12BIT BIN CTR(MO,FC)	965-587-46	1	Z18
13	IC, 4556 DUAL 10F4 DEC(MO,FC,NL	965-587-48	1	Z1
14	IC, 4555 DUAL 10F4 NI(MO,FC,NL	965-587-68	1	Z14
15	IC, 301A OPAMP(8DIP)(NL,SG)	965-592-01	1	Z11
16	IC, LF351N FET OP AMP(NL)	965-616-01	2	Z16,Z19
17	IC, 4572 INV,NOR,NAND CMOS (MO)	965-618-00	2	Z3,Z15
18	IC, LM329BZ 20PPM REF (NL)	965-636-00	1	Z20
19	IC, LM78L15ACZ 15V REG92(NL)	965-637-00	1	Z21
20				
21				
22				
23				
24				

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, REED FEM	MODEL NO. 235	230-4410-03	E
		DATE 3-17-89	SHEET 4 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN60C, 499K	920-449-93	1	R79
26	RES, FILM RN55D 1% 10K	924-310-02	1	R56
27	RES, FILM RN55C 2K	924-420-01	2	R53-54
28	RES, FILM RN55C 6.98K	924-469-81	1	R44
29	RES, FLAMEPROOF 1/4W ±5%, 10	940-001-00	3	R58,R59,R98
30	RES, CARBON 1/4W ± 5%, 100	942-201-01	3	R94,R95,R97
31				
32	RES, CARBON 1/4W ± 5%, 10K	942-201-03	3	R60,R68,R85
33	RES, CARBON 1/4W ± 5%, 100K	942-201-04	7	R62,R73,R87-88 R92,R102,R104
34	RES, CARBON 1/4W ± 5%, 10M	942-201-06	2	R99,R105
35				
36	RES, CARBON 1/4W ± 5%, 150	942-201-51	2	R52,R82
37	RES, CARBON 1/4W ± 5%, 15K	942-201-53	1	R91
38	RES, CARBON 1/4W ± 5%, 20K	942-202-03	9	R45-46,R49-51,57 R66-67,R74
39	RES, CARBON 1/4W ± 5%, 220	942-202-21	2	R80,R96
40	RES, CARBON 1/4W ± 5%, 220K	942-202-24	2	R81,R83
41	RES, CARBON 1/4W ± 5%, 270	942-202-71	1	R84
42	RES, CARBON 1/4W ± 5%, 33K	942-203-33	1	R69
43	RES, CARBON 1/4W ± 5%, 3.9K	942-203-92	1	R48
44	RES, CARBON 1/4W ± 5%, 39K	942-203-93	4	R47,R71-72,R86
45	RES, CARBON 1/4W ± 5%, 470	942-204-71	1	R70
46	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	1	R101
47	RES, CARBON 1/4W ± 5%, 47K	942-204-73	2	R89,R90
48	RES, CARBON 1/4W ± 5%, 680	942-206-81	1	R61

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, REED FEM	MODEL NO. 235	230-4410-03	E
		DATE 3-17-80	SHEET 5 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	RES, CARBON 1/2W ± 5%, 2.2K	942-302-22	40	R1-40
50				
51				
52				
53				
54	CAP, TANT, 4.7 @ 35V (1960)	916-470-35	1	C71
55	CAP, DISC .01/500V (5GA)	900-021-04	8	C65,C67,C70, C73-75,C85-86
56	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	2	C76,C78
57	CAP, DISC, 100 PF @ 1 KV (5GA)	901-011-01	45	C1-40,C62-63, C77,C83,C87
58	CAP, PLP,/.1/200V,IMB(GA2C104K)	917-001-20	1	C79
59	CAP, PLP,.22/200V,IMB(GA2C224K)	917-022-20	2	C82,C84
60	CAP, PLP,.47/200V,IMB(GA2C474K)	917-047-20	2	C66,C68
61	CAP, SF, .1/100V,SMS(B32570)	918-001-10	3	C69,C72,C81
62	CAP, SF, .0022/250V, SMS(B32570)	918-002-25	1	C64
63	CAP,SF, .22/100V, SMS (B32570)	918-022-10	1	C80
64				
65				
66				
67				
68				
69	DIODE, 1N914 (1N4148)(RD,FC,TI	961-091-40	11	CR4-10,CR13, CR14,CR16,CR17
70	DIODE, 1N5229B 4.3V (MO)	961-522-92	1	CR3
71				
72	DIODE, IN5240, 10V	961-524-00	2	CR11,CR12

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
PCB ASSEMBLY, REED FEM	MODEL NO. 235	DATE 3-17-80	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74				
75				
76				
77	TRANSISTOR(SELECTED-COLOR DOT)	220-7200-01	1	Q1
78	GRADED 4016	000-7700-00	4	Z6,Z9-10,Z12
79	RELAY, REED LOW THERMAL	000-8043-00	20	K1-20
80	FET, 2202 (NJ,LO-LK,GP)	100-722-02	4	Q14,Q16,Q17,Q2
81	TRANSFORMER, INTERFACE	230-7030-00	1	T1
82	RESISTOR NETWORK, FEM	230-7100-00	1	RN1
83	POT, 1K VISHAY (1280)	960-011-30	1	R63
83	POT, 100 CERMET (72PL)	960-015-19	1	R55
84	POT, 25K MT2X253	960-015-15	2	R43,R100
85	XSTR, PN2222 (NPNA92)(NA)	962-222-20	3	Q8,Q9,Q11
86	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	6	Q3-4,Q7,Q10, Q13,Q15
87	FET, NP05566(NJ,LO,NSB,8BTT)NL	962-556-60	1	Q5
88	XSTR, MPSA13 (NPNA/DRL92)(M)	964-040-03	2	Q6,Q12
89	OPTO, FCD8316 (FC)	965-570-03	2	OC1,OC2
90	T.S 20P ELCTVT 8145 251352053	973-010-55	2	
91	SPACER, 1/8X6A2(L6310-2-2A)	991-020-88	2	
92	DISS-O-PAD .250 O.D. X .125 I.D. X .03 BIVAR INC TO-16-03	979-020-11	6	

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, CURRENT XMTR	MODEL NO. 235	230-4411-03	E
		DATE 3-17-80	SHEET 3 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB REED FEM	230-2410-02	1	
2	SCHEMATIC	231-6411-03	1	
3	TEST SPEC		1	
4				
5				
6	IC, LM393 DUAL COMP(8DIP)(NL)	965-580-00	1	Z4
7	IC, 4001 4-2IN NOR CMOS(MO)	965-587-01	1	Z17
8	IC, 4015 DUAL SR CMOS (MO)	965-587-03	1	Z7
9	IC, GRADED 4066	000-8130-00	1	Z13
10	IC, 4013 DUAL D FF CMOS(FC,MO)	965-587-23	1	Z8
11	IC, 74C42 BCD-DECIMAL DEC CMOS	965-587-34	2	Z2,Z5
12	IC, 4040 12BIT BIN CTR(MO,FC)	965-587-46	1	Z18
13	IC, 4556 DUAL 10F4 DEC(MO,FC,NL	965-587-48	1	Z1
14	IC, 4555 DUAL 10F4 NI(MO,FC,NL	965-587-68	1	Z14
15	IC, 301A OPAMP(8DIP)(NL,SG)	965-592-01	1	Z11
16	IC, LF351N FET OP AMP(NL)	965-616-01	2	Z16,Z19
17	IC, 4572 INV,NOR,NAND CMOS (MO)	965-618-00	2	Z3,Z15
18	IC, LM329BZ 20PPM REF (NL)	965-636-00	1	Z20
19	IC, LM78L15ACZ 15V REG92(NL)	965-637-00	1	Z21
20				
21				
22				
23				
24				

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

EMERSON

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, CURRENT XMTR.	MODEL NO. 235	230-4411-03	E
		DATE 3-17-89	SHEET 4 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN60C, 499K	920-449-93	1	R79
26	RES, FILM RN55D 1% 10K	924-310-02	1	R56
27	RES, FILM RN55C 2K	924-420-01	2	R53,R54
28	RES, FILM RN55C 6.98K	924-469-81	1	R44
29	RES, FLAMEPROOF 1/4W ±5%, 10	940-001-00	3	R58,R59,R98
30	RES, CARBON 1/4W ± 5%, 100	942-201-01	3	R94,R95,R97
31				
32	RES, CARBON 1/4W ± 5%, 10K	942-201-03	3	R60,R68,R85
33	RES, CARBON 1/4W ± 5%, 100K	942-201-04	7	R62,R73,R87-88, R92,R102,R104
34	RES, CARBON 1/4W ± 5%, 10M	942-201-06	2	R99,R105
35				
36	RES, CARBON 1/4W ± 5%, 150	942-201-51	2	R52,R82
37	RES, CARBON 1/4W ± 5%, 15K	942-201-53	1	R91
38	RES, CARBON 1/4W ± 5%, 20K	942-202-03	9	R45-46,R49-51,57 R66-67,R74
39	RES, CARBON 1/4W ± 5%, 220	942-202-21	2	R80,R96
40	RES, CARBON 1/4W ± 5%, 220K	942-202-24	2	R81,R83
41	RES, CARBON 1/4W ± 5%, 270	942-202-71	1	R84
42	RES, CARBON 1/4W ± 5%, 33K	942-203-33	1	R69
43	RES, CARBON 1/4W ± 5%, 3.9K	942-203-92	1	R48
44	RES, CARBON 1/4W ± 5%, 39K	942-203-93	4	R47,R71-72,R86
45	RES, CARBON 1/4W ± 5%, 470	942-204-71	1	R70
46	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	1	R101
47	RES, CARBON 1/4W ± 5%, 47K	942-204-73	2	R89,R90
48	RES, CARBON 1/4W ± 5%, 680	942-206-81	1	R61

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, CURRENT XMTR.	MODEL NO. 235	DATE 3-17-80	SHEET 5 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	RES, WW, .1%, 20	938-002-00	20	R1-20
50				
51				
52				
53				
54	CAP, TANT 4.7 @ 35V (1960)	916-470-35	1	C71
55	CAP, DISC .01/500V (5GA)	900-021-04	8	C65,C67,C70, C73-75,C85-86
56	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	2	C76,C78
57	CAP, DISC, 100 PF @ 1 KV (5GA)	901-011-01	45	C1-40,C62-63, C77,C83,C87
58	CAP, PLP,/.1/200V,IMB(GA2C104K)	917-001-20	1	C79
59	CAP, PLP,.22/200V,IMB(GA2C224K)	917-022-20	2	C82,C84
60	CAP, PLP,.47/200V,IMB(GA2C474K)	917-047-20	2	C66,C68
61	CAP, SF, .1/100V,SMS(B32570)	918-001-10	3	C69,C72,C81
62	CAP, SF, .0022/250V, SMS(B32570)	918-002-25	1	C64
63	CAP,SF, .22/100V, SMS(B32570)	918-022-10	1	C80
64				
65				
66				
67				
68				
69	DIODE, 1N914 (1N4148)(RD,FC,TI	961-091-40	11	CR4-10,CR13, CR14,CR16,CR17
70	DIODE, 1N5229B 4.3V (MO)	961-522-92	1	CR3
72	DIODE, IN5240, 10V	961-524-00	2	CR11,CR12

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, CURRENT XTRM.	MODEL NO. 235	230-4411-03	E
		DATE 3-17-80	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74				
75				
76				
77	TRANSISTOR(SELECTED-COLOR DOT)	220-7200-01	1	Q1
78	GRADED 4016	000-7700-00	4	Z6,Z9,Z10,Z12
79	RELAY, REED LOW THERMAL	000-8043-00	20	K1-20
80	FET, 2202 (NJ,LO-LK,GP)	100-722-02	4	Q14,Q16-17,Q2
81	TRANSFORMER, INTERFACE	230-7030-00	1	T1
82	RESISTOR NETWORK, FEM	230-7100-00	1	RN1
83	POT, 1K VISHAY (1280)	960-011-30	1	R63
83	POT, 100 CERMET (72PL)	960-015-19	1	R55
84	POT, 25K MT2X253	960-015-15	2	R43,R100
85	XSTR, PN2222 (NPNA92)(NA)	962-222-20	3	Q8,Q9,Q11
86	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	6	Q3-4,Q7,Q10,Q13 Q15
87	FET, NP05566(NJ,LO,NSB,8BTT)NL	962-556-60	1	Q5
88	XSTR, MPSA13 (NPNA/DRL92)(M)	964-040-03	2	Q6,Q12
89	OPTO, FCD8316 (FC)	965-570-03	2	OC1,OC2
90	T.S 20P ELCTVT 8145 251352053	973-010-55	2	
91	SPACER, 1/8X6A2(L6310-2-2A)	991-020-88	2	
92	DISS-O-PAD .250 O.D. X .125 I.D. X .03 BIVAR INC TQ-16-03	979-020-11	6	
93	JUMPER J.600 X .125 T22	991-010-06	1	

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, HIGH VOLTAGE	MODEL NO. 235	230-4412-02	U
		DATE 3-17-80	SHEET 3 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB REED FEM	230-2410-02	1	
2	SCHEMATIC	231-6410-02	1	
3	TEST SPEC		1	
4				
5				
6	IC, LM393 DUAL COMP(8DIP)(NL)	965-580-00	1	Z4
7	IC, 4001 4-2IN NOR CMOS(MO)	965-587-01	1	Z17
8	IC, 4015 DUAL SR CMOS (MO)	965-587-03	1	Z7
9	IC, GRADED 4066	000-8130-00	1	Z13
10	IC, 4013 DUAL D FF CMOS(FC,MO)	965-587-23	1	Z8
11	IC, 74C42 BCD-DECIMAL DEC CMOS	965-587-34	2	Z2,Z5
12	IC, 4040 12BIT BIN CTR(MO,FC)	965-587-46	1	Z18
13	IC, 4556 DUAL 10F4 DEC(MO,FC,NL	965-587-48	1	Z1
14	IC, 4555 DUAL 10F4 NI(MO,FC,NL	965-587-68	1	Z14
15	IC, 301A OPAMP(8DIP)(NL,SG)	965-592-01	1	Z11
16	IC, LF351N FET OP AMP(NL)	965-616-01	2	Z16,Z19
17	IC, 4572 INV,NOR,NAND CMOS (MO)	965-618-00	2	Z3,Z15
18	IC, LM329BZ 20PPM REF (NL)	965-636-00	1	Z20
19	IC, LM78L15ACZ 15V REG92(NL)	965-637-00	1	Z21
20				
21				
22				
23				
24				

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, HIGH VOLTAGE	MODEL NO. 235	230-4412-02	U
		DATE 3-17-89	SHEET 4 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN60C, 499K	920-449-93	1	R79
26	RES, FILM RN55D 1% 10K	924-310-02	1	R56
27	RES, FILM RN55C 2K	924-420-01	2	R53,R54
28	RES, FILM RN55C 6.98K	924-469-81	1	R44
29	RES, FLAMEPROOF 1/4W ±5%, 10	940-001-00	3	R58,R59,R98
30	RES, CARBON 1/4W ± 5%, 100	942-201-01	2	R94,R95
31				
32	RES, CARBON 1/4W ± 5%, 10K	942-201-03	4	R60,R68,R85,R99
33	RES, CARBON 1/4W ± 5%, 100K	942-201-04	7	R62,R73,R87-88 R92,R102,R104
34	RES, CARBON 1/4W ± 5%, 10M	942-201-06	1	,R105
35				
36	RES, CARBON 1/4W ± 5%, 150	942-201-51	2	R52,R82
37	RES, CARBON 1/4W ± 5%, 15K	942-201-53	1	R91
38	RES, CARBON 1/4W ± 5%, 20K	942-202-03	9	R45-46,R49-51,57 R66-67,R74
39	RES, CARBON 1/4W ± 5%, 220	942-202-21	2	R80,R96
40	RES, CARBON 1/4W ± 5%, 220K	942-202-24	2	R81,R83
41	RES, CARBON 1/4W ± 5%, 270	942-202-71	1	R84
42	RES, CARBON 1/4W ± 5%, 33K	942-203-33	1	R69
43				
44	RES, CARBON 1/4W ± 5%, 39K	942-203-93	3	R71-72,R86
45	RES, CARBON 1/4W ± 5%, 470	942-204-71	1	R70
46				
47	RES, CARBON 1/4W ± 5%, 47K	942-204-73	2	R89,R90
48	RES, CARBON 1/4W ± 5%, 680	942-206-81	1	R61

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, HIGH VOLTAGE	MODEL NO. 235	230-4412-02	U
		DATE 3-17-80	SHEET 5 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	RES, CARBON 1/2W ± 5%, 2.2K	942-302-22	40	R1-R40
50	RES, FILM RN55C, 909K 1%	924-490-93	1	R101
51	RES, 0.1%, 9M (CADDOCK MK132)	922-590-04	1	R106
52	RES, 0.1%, 1M (CADDOCK MK632)	922-510-04	1	R107
53				
54	CAP, TANT 4.7 @ 35V (1960)	916-470-35	1	C71
55	CAP, DISC .01/500V (5GA)	900-021-04	6	C70 ,C73-75, C85,C86
56	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	2	C76,C78
57	CAP, DISC, 100 PF @ 1 KV (5GA)	901-011-01	45	C1-40,C62-63, C77,C83,C87
58	CAP, PLP,/.1/200V,IMB(GA2C104K)	917-001-20	1	C79
59	CAP, PLP,.22/200V,IMB(GA2C224K)	917-022-20	2	C82,C84
60				
61	CAP, SF, .1/100V,SMS(B32570)	918-001-10	3	C69,C72,C81
62	CAP, SF, .0022/250V, SMS(B32570)	918-002-25	1	C64
63	CAP,SF, .22/100V, SMS(B32570)	918-022-10	1	C80
64				
65				
66				
67				
68				
69	DIODE, 1N914 (1N4148)(RD,FC,TI	961-091-40	12	CR4-10,CR13-17
70	DIODE, 1N5229B 4.3V (MO)	961-522-92	1	CR3
71				
72	DIODE, IN5240, 10V	961-524-00	2	CR11,CR12

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

EMERSON

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, HIGH VOLTAGE	MODEL NO. 235	230-4412-02	U
		DATE 3-17-80	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74				
75				
76				
77	TRANSISTOR(SELECTED-COLOR DOT)	220-7200-01	1	Q1
78	GRADED 4016	000-7700-00	4	Z6,Z9,Z10,Z12
79	RELAY, REED LOW THERMAL	000-8043-00	20	K1-K20
80	FET, 2202 (NJ,LO-LK,GP)	100-722-02	3	Q14,Q16,Q17
81	TRANSFORMER, INTERFACE	230-7030-00	1	T1
82	RESISTOR NETWORK, FEM	230-7100-00	1	RN1
83	POT, 1K VISHAY (1280)	960-011-30	1	R63
83	POT, 100 CERMET (72PL)	960-015-19	1	R55
84	POT, 25K MT2X253	960-015-15	2	R100, R43
85	XSTR, PN2222 (NPNA92)(NA)	962-222-20	3	Q8,Q9,Q11
86	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	6	Q3-4,Q7,Q10-11, Q15
87	FET, NP05566(NJ,LO,NSB,8BTT)NL	962-556-60	1	Q5
88	XSTR, MPSA13 (NPNA/DRL92)(M)	964-040-03	2	Q6,Q12
89	OPTO, FCD8316 (FC)	965-570-03	2	OC1,OC2
90	T.S 20P ELCTVT 8145 251352053	973-010-55	2	
91	SPACER, 1/8X6A2(L6310-2-2A)	991-020-88	2	
92	DISS-O-PAD .250 O.D. X .125 I.D. X .03 BIVAR INC TO-16-03	979-020-11	6	

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY RTD FEM	MODEL NO. 235	DATE 3-18-80	SHEET 3 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, RTD MULTIPLEXER	230-2430-02	1	
2	SCHEMATIC	231-6430-01	1	
3	TEST SPEC		1	
4				
5				
6	IC, LM393 DUAL COMP(8DIP)(NL)	965-580-00	1	Z21
7	IC, 4001 4-2IN NOR CMOS (MO)	965-587-01	1	Z32
8	IC, 4011 4-2IN NAND CMOS (MO)	965-587-02	1	Z25
9	IC, 4015 DUAL SE CMOS (MO)	965-587-03	1	Z18
10	IC, GRADED 4066	000-8130-00	1	Z31
11	IC, 4013 DUAL D FF CMOS (FC,MO)	965-587-23	1	Z22
12	IC, 74C42 BCD-DECIMAL DEC CMOS	965-587-34	1	Z19
13	IC, 4040 12BIT BIN CTR(MO,FC)	965-587-46	1	Z33
14	IC, 301A OPAMP(8DIP)(NL,SG)	965-592-01	1	Z34
15	IC, LF351N FET OP AMP (NL)	965-616-01	2	Z27,Z28
16	IC, 4572 INV, NOR, NAND CMOS(MO)	965-618-00	1	Z26
17	IC, LM8L15ACZ 15V REG92(NL)	965-637-00	2	Z16,Z17
18				
19				
20				
21				
22				
23	RES, FILM RN60C, 499K	920-449-93	1	R79
24	RES, FILM RN55D 1% 10K	924-310-02	1	R56

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY RTD FEM	MODEL NO. 235	DATE 3-18-80	SHEET 4 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, FILM RN55D 1.43K	924-314-30	1	R65
26	RES, FILM RN55D 19.6K	924-319-62	1	R89
27	RES, FILM RN55D 1% 20K	924-320-02	2	R87,R92
28	RES, FILM RN55D 3.16K	924-331-61	1	R77
29	RES, FILM RN55D 40.2K	924-340-22	1	R91
30	RES, FILM RN55D 4.64K	924-346-41	1	R98
31	RES, FILM RN55D 5.36K	924-353-62	1	R76
32	RES, FILM RN55D 6.81K	924-368-12	1	R64
33	RES, FILM RN55D 7.23K	924-372-32	1	R86
34	RES, FILM RN55D 86.6K	924-386-62	1	R75
35	RES, FILM RN55C 2K	924-420-01	2	R53,R54
36	RES, FILM .01% W/W 225 (E1TYPE27)	937-201-28	1	R103
37	RES, CARBON 1/4W ± 5%, 100	942-201-01	2	R58,R59
38	RES, CARBON 1/4W ± 5%, 1K	942-201-02	2	R41,R42
39	RES, CARBON 1/4W ± 5%, 10K	942-201-03	2	R60,R68
40	RES, CARBON 1/4W ± 5%, 100K	942-201-04	9	R62,R73,R84,R93, R95,R99-102
41	RES, CARBON 1/4W ± 5%, 15	942-201-50	1	R169
42	RES, CARBON 1/4W ± 5%, 150	942-201-51	2	R52,R82
43	RES, CARBON 1/4W ± 5%, 15K	942-201-53	1	R97
44	RES, CARBON 1/4W ± 5%, 30K	942-203-03	1	R165
45	RES, CARBON 1/4W ± 5%, 20K	942-202-03	10	R45-46,R49-51,57 R66-67,R74,R164
46	RES, CARBON 1/4W ± 5%, 220	942-202-21	2	R80,R171
47	RES, CARBON 1/4W ± 5%, 220K	942-202-24	2	R81,R83
48	RES, CARBON 1/4W ± 5%, 33K	942-203-33	1	R69

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DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

EMERSON

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY RTD FEM	MODEL NO. 235	230-4430-01	P.
		DATE 3-18-80	SHEET 5 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	RES, CARBON 1/4W ± 5%, 3.9K	942-203-92	1	R48
50	RES, CARBON 1/4W ± 5%, 39K	942-203-93	4	R47,R71,R72,R85
51	RES, CARBON 1/4W ± 5%, 470	942-204-71	1	R70
52	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	1	R170
53	RES, CARBON 1/4W ± 5%, 47K	942-204-73	2	R94,R96
54	RES, CARBON 1/4W ± 5%, 51	942-205-10	1	R168
55	RES, CARBON 1/4W ± 5%, 680	942-206-81	1	R61
56	RES, CARBON 1/4W ± 5%, 8.2K	942-208-22	1	R90
57	RES, CARBON 1/2W ± 5%, 2.2K	942-302-22	100	R1-40,R104-163
58	RES, CARBON 1/4W ± 5%, 1M	942-201-05	1	R174
59	RES, FLAMEPROOF 1/4W ±5%, 10	940-001-00	1	R172
60				
61				
62	CAP, TANT, 4.7 @ 35V (1960)	916-470-35	1	C71
63	CAP, DISC, .01 @ 500V (5GA)	900-021-04		C1-40,70,73-75, 61,65,67,86
64	CAP, DISC, .001 @ 1KV (5GA)	900-081-03	3	C76,C78,C85
65	CAP, DISC, 100 PF @ 1KV (5GA)	901-011-01	6	C62,C63,C77,C83, C84,C88
66	CAP,PLP,/.1/200V,IMB(GA2C104K)	917-001-20	1	C79
67	CAP,PLP,.22/200V,IMB(GA2C224K)	917-022-20	1	C82
68	CAP,PLP,.47/200V,IMB(GA2C474K)	917-047-20	2	C66,C68
69	CAP, SF, .1/100V, SMS(B32570)	918-001-10	4	C72,C69,C81,C87
70	CAP, SF, .0022/250V,SMS(B32570)	918-002-25	1	C64
71	CAP, SF, .22/100V, SMS(B32570)	918-022-10	21	C41-60,C80
72				

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123
EMERSON

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY RTD FEM	MODEL NO. 235	230-4430-01	P
		DATE 3-18-80	SHEET 6 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
73				
74				
75				
76				
77	DIODE, 1N914 (1N4148)(TD,FC,TI	961-091-40	12	CR4-13,CR15-16
78	DIODE, 1N5229B 4.3V (MO)	961-522-92	1	CR3
79	DIODE, 1N5236B (7.5V)	961-523-62	2	CR2,CR14
80	DIODE, 1N5237B 8.2V (MO)	961-523-72	1	CR1
81				
82				
83				
84				
85				
86	GRADED 4016	000-7700-00	4	Z23-24,Z29-30
87	SELECTED 4052 CMOS MULTI	000-8051-00	16	Z1-15,Z20
88	FET, 2202 (NJ,L)-LK,GP)	100-722-02	2	Q2,Q14
89	XFMR. RTD INTERFACE	230-7060-00	1	T1
90	POT, 1K CERMET (89PR)	960-011-02	1	R88
91	POT, 100 CERMET (72XL)	960-011-17	1	R55
92	POT, 500 CERMET (72XL)	960-015-07	1	R167
93	POT, 50K CERMET (72XL)	960-015-08	1	R166
94	POT, 25K CERMET (72XL)	960-015-10	1	R173
95	XSTR, PN2222 (NPNA92)(NA)	962-222-20	6	Q1,Q8,Q9,Q11, Q17,Q18
96	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	7	Q3-4,Q10,Q13, Q7,Q15-16

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY RTD FEM	MODEL NO. 235	230-4430-01	P
		DATE 3-18-80	SHEET 7 OF 7

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
97	FET, NPD5566(NJ,LO,NSE,8BIT)NL	962-556-60	1	Q5
98	XSTR, MPSA13 (NPNA/DRL92)(M)	964-040-03	2	Q6,Q12
99	OPTO, FCD831B (FC)	965-570-03	2	OC1,OC2
100	T.S 20P ELCTVT 8145 251352053	973-010-55	4	
101	STDF, 5/8X440 A2(L6911-10-2A)	991-020-85	4	
102	SPACER, 1/8X6A2(L6310-2-2A)	991-020-88	3	
103	IC SOCKET, 16DIP LP (516AG11D)	992-010-10	16	
104	FLAT CBL, 3(ANSLEY FSN-23A-24)	993-100-07	1	
105	WASHER, SPLITLOCK 4	986-200-04	4	
106	WASHER, FLAT 4	986-100-04	4	
107	SCREW, PAN HD. PHILLIPS, 4-40 X 5/16"	980-440-031	4	
108	DISS-O-PAD .025 O.D. X .125 I.D. X .03 BIVAR INC TO-16-03	979-020-11	12	

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, ALARM BOARD	MODEL NO. 235	231-4360-01	D
		DATE 2-27-80	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, ALARM BOARD	231-2360-02	1	
2	SCHEMATIC	231-6360-01	1	
3	TEST SPEC			
4				
5				
6	IC, 74C14 HEX INV CMOS	965-587-60	2	4M,4N
7	IC, 8T97	965-643-01	1	5A
8	IC, 74LS374 OCTAL D LATCH	965-587-74	5	1H-5H
9	IC, 4334-3 1KX4 CMOS RAM	965-613-13	4	2B,2C,2D,2E
10	IC, 74LS86 EXCL-OR	965-635-32	1	5E
11	IC, 74LS04 HEX INV (FC,MO,NL)	965-635-00	4	2A,3A,4A,5D
12	IC, 74LS245 8 BUS XCVR(TI,FC)	965-635-04	1	1A
13	IC, 74LS00 4-2IN NAND (TI)	965-635-07	2	3E,5M
14	IC, 74LS10 3-3IN NAND (TI)	965-635-08	3	4D,4E,4F
15	IC, 74LS30 1-8IN NAND (TI)	965-635-10	1	4B
16	IC, 74LS02 QUAD 2 IN NOR	965-635-17	3	3D,4C,5N
17	IC, 74LS74 DUAL D F/F	965-635-19	3	5B,5K,5L
18	IC, 74LS138 3-8 DEC/MUX	965-635-22	1	3C
19	IC, 74LS27 3-3IN POS-NOR(TI,FC)	965-635-25	1	3B
20	IC, 74LS175 QUAD D F/F	965-635-46	1	5C
21	IC, 74LS244 BUS BUFFER	965-635-03	1	5J
22				
23				
24				

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB, ALARM BOARD	MODEL NO. 235	DATE 2-27-80	SHEET 4 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25				
26	RES, CARBON 1/4W ±5%, 1K	942-201-02	2	R11,12
27	RES, CARBON 1/4W ±5%, 10K	942-201-03	5	R7-10, R4
28	RES, CARBON 1/4W ±5%, 220	942-202-21	1	R5
29	RES, CARBON 1/4W ±5%, 330K	942-203-34	1	R6
30	RES, CARBON 1/4W ±5%, 680	942-206-81	2	R2,3
31	RES, NETWK 10K SIP (785-1-R10K)	952-010-02	3	RN3,RN2, RN8
32	RES, NTWK, 470 DIP (898-3-R470)	950-047-00	4	RN7,RN4,RN5,RN6
33	RES, CARBON 1/4W ±5%, 3.3K	942-203-32	1	R1
34	RES, NETWK, 1K SIP (785-3-R1K)	952-010-01	1	RN1
35	RES, CARBON 1/4W ±5%, 10K	942-201-03	1	R13
36	RES, CARBON 1/4W ±5%, 390	942-203-91	1	R14
37				
38	CAP, AXIAL .01/50V 180/Z5V050A	900-021-07	18	C3,5,7,9-23
39	CAP, DISC, 100PF @ 1KV (5GA)	901-011-01	3	C1,2,25
40	CAP, TANT, 10 @ 10V	916-010-10	4	C4,6,8,24
41	CAP, DISC .01 @ 500V	900-021-04	1	C26
42				
43				
44				
45				
46	DIODE, 1N914 (1N4148)(TD,FC,TI)	961-091-40	14	CR1-14
47	XSTR, 2N3646 (NPNSH106)(MO,FC)	962-364-64	2	Q1-2
48	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	2	Q4-5

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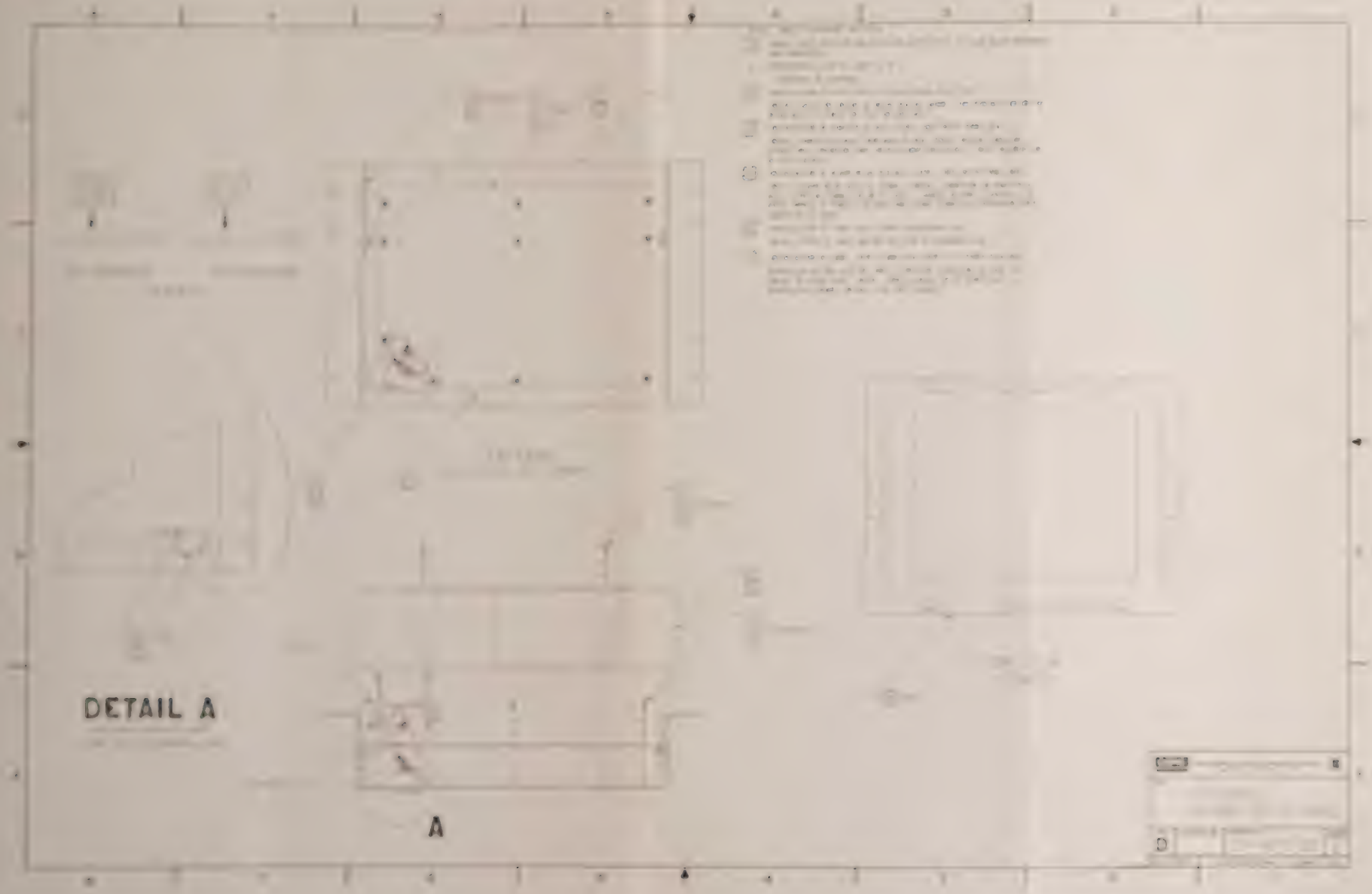
MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY, PCB, ALARM BOARD	MODEL NO. 235	231-4360-01	D
	DATE 2-27-80	SHEET 5 OF 5	

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	XSTR, MPSA13 (NPNA/DRL92)(M)	964-040-03	1	Q3
50	OPTO ISO-DUAL (LIT-ILCT6)	000-7540-00	22	1KA,B-4KA, B,1LA,B-4LA,B,1M,A,B,-3M,A,B
51	XSTR, PN2222	962-222-20	1	Q6
52	SWITCH, DIP3P (GH76SCO3S)	969-050-17	1	S3
53	SWITCH, ALCO TPA11FG-PC-2	969-050-16	1	S2
54	CHASSIS FASTENER 632B2 US1590B1	991-020-26	1	
55				
56	CONN, PC37 PIN (F)(AMP745108-2)	973-010-78	2	J1,2
57				
58	BATT 2.4V GE41B901BE11G1	975-100-08	1	BT 1 Install at test level
59	SCREW, PAN HD PHILLIPS 4-40 X 3/8 LG	980-440-038	4	J1,2
60	NUT, RADIAL 4-40	984-200-440	4	J1,2
61	WASHER, SPLITLOCK #4	986-200-04	4	J1,2
62	WASHER, FLAT NO. 4	986-100-04	4	J1,J2
63	SCREW PHMS 6-32 X 1/2 LG	980-632-050	1	
64	WASHER, FLAT #6	986-100-06	1	
65	WASHER, SPLITLOCK #6	986-200-06	1	
66				
67				
68				
69				
70				
71				
72				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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY, ALARM RELAY PANEL	MODEL NO. 235 RELAY PANEL	231-4270-00	E
		DATE 6-13-80	SHEET 2 OF 2

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	ASSEMBLY, PCB, ALARM RELAY	231-4370-00	1	
2	ASSEMBLY, POWER PLUG	231-4070-00	1	
3	PANEL, RELAY BOX	231-2270-00	1	
4	COVER, RELAY PANEL	230-2290-00	1	
5	GATE, RELAY PANEL	230-2270-01	2	
6	SCREW, PAN HD• PHIL. 10-32 X 1/2	980-1032-050	2	
7	SCREW, PAN HD• PHIL. 4-40 X 3/8	980-440-038	10	
8	SCREW, PAN HD• PHIL. 6-32 X 3/8	980-632-038	4	
9	WASHER, SPLIT LOCK 10	986-200-10	2	
10	WASHER, SPLIT LOCK 4	986-200-04	10	
11	WASHER, FLAT 4	986-100-04	10	
12	WASHER, FLAT 10	986-100-10	2	
13	WASHER, FLAT 6	986-100-06	4	
14	WASHER, SPLITLOCK 6	986-200-06	4	
15	LABEL, 115/220 VAC	231-2162-00	1	
16	SHIPPING CONTAINER	999-000-03	1	NOT SHOWN
17	FUSE, 1/8 AMP SLO-BLOW	971-000-05	1	
18	POWER CORD	993-200-07	1	NOT SHOWN
19	ASSEMBLY, CABLE INTER-CONNECT	231-5450-00	1	NOT SHOWN
20	OUTLINE DRAWING, ASSEMBLY RELAY PANEL	231-8030-00	1	
21	COVER, PLATE, POWER PLUG	231-2950-00	1	
22	STANDOFF, HEX, MALE/FEMALE	991-021-18	2	

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, ALARM RELAY PANEL	MODEL NO. 235	DATE 4	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, RELAY PANEL	231-2370-00	1	
2	SCHEMATIC	231-6370-00	1	
3	TEST SPEC		1	
4				
5				
6	IC, 555 TIMER	965-586-00	1	Z1
7	IC, 74LS393	965-635-06	1	Z7
8	IC, 74LS138	965-635-22	3	Z3-5
9	IC, 74C14	965-587-60	3	Z12,14,16
10	IC, ULN2003A	965-625-01	3	Z13,15,17
11	IC, 6N138 OPTO	965-570-01	1	Z9
12	IC, 74LS175	965-635-46	1	Z6
13	IC, 74LS00	965-635-07	1	Z2
14	IC, 74LS174	965-635-23	1	Z11
15	IC, 74LS04	965-635-00	2	Z8,Z10
16				
17				
18				
19	RES, CARBON 1/4W ± 5%, 10 Ω	942-201-00	1	R11
20	RES, CARBON 1/4W ± 5%, 1K	942-201-02	1	R12
21	RES, CARBON 1/4W ± 5%, 220	942-202-21	1	R8
22	RES, CARBON 1/4W ± 5%, 3.3K	942-203-32	1	R7
23	RES, CARBON 1/4W ± 5%, 390	942-203-91	4	R3··R6
24	RES, CARBON 1/4W ± 5%, 51K	942-205-13	2	R1,R2

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, ALARM RELAY PANEL	MODEL NO. 235	231-4370-01	B
		DATE 4	SHEET 4 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES NTWK SIP 785-1-R10K	952-010-02	2	RN2,RN4
26	RES NTWK DIP 898-3-R220	951-022-00	2	RN1,3
27	RES NTWK DIP 898-3-R470	950-047-00	3	RN5,6,7
28	RES, CARBON 1/4W ±5%, 470	942-204-71	2	R9,R10
29	RES, CARBON 1/4W ±5%, 330K	942-203-34	1	R13
30	CAP .01 UF 50V (1801Z5U050A)	900-021-07	34	C1,2,4-20,22, 24-32,35-38,39
31	CAP 1UF TANT 50V (196D)	916-010-05	1	C21
32	CAP 10UF TANT 35V (196D)	916-010-35	2	C33,C34
33	CAP 1800UF ELECT 30V (39D)	910-180-30	1	C23
34	CAP 10UF TANT 10V (162D)	916-010-10	1	C3
35	CAP, DISC, .01 @ 500V (5GA)	900-021-04	1	C40
36				
37				
38				
39	DIODE 1N4002 100V 1A	966-002-00	5	CR18-22
40	DIODE 1N914 (1N4148)	961-091-40	17	CR1-17
41				
42				
43				
44				
45				
46	REGULATOR, 7805 (5V)	965-551-00	1	Z18
47	HEATSINK, THERMALLOY THM6073	991-008-00	1	
48	XFORMER, POWER 115/230VAC	400-7040-01	1	T1

ML

MATERIAL LIST

[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	97[illegible]	1	[illegible]
[illegible]	[illegible], FEMALE [illegible] 20301[illegible])	971-010-5[illegible]	8	
[illegible]	RELAY SOCKET [illegible]	[illegible]	16	
[illegible]	RELAY RETAINER [illegible] ST 100-1)	971-010-91	16	
[illegible]	TERMINAL BLOCK, 16T [illegible]	971-010-6[illegible]	1	TB[illegible]
[illegible]	TERMINAL BLOCK, 10T [illegible]	971-010-0[illegible]	4	TB[illegible]
[illegible]	TERMINAL BLOCK [illegible]	[illegible]	1	[illegible]
[illegible]	[illegible]	[illegible]	1	[illegible]
[illegible]	SCREW #6-32 X [illegible]	900-612-0[illegible]	1	
[illegible]	SCREW #4-40 X 1 1/4 LG	[illegible]	[illegible]	
[illegible]	WASHER, SPLITLOCK #6	906-[illegible]-06	1	
[illegible]	NUT, HEX #4-40	906-100-44[illegible]	2	
[illegible]	NUT, RADIAL #6-32	906-200-632	1	
[illegible]	WASHER, SPLITLOCK #4	906-200-04	2	

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
PCB ASSEMBLY, MEMORY EXTENSION "D"	MODEL NO. 235	DATE 1-19-82	SHEET 3 OF 5
		231-4462-00	D

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, MEMORY EXTENSION B'D "D"	231-2462-00	1	
2	SCHEMATIC	231-6462-00	1	
3	TEST SPEC		1	
4				
5				
6	IC, 74LS00	965-635-07	1	4D
7	IC, 74LS02	965-635-17	2	1C,2C
8	IC, 74LS175	965-635-46	1	4C
9	IC, 74LS10	965-635-08	4	2B,1D,2D,3D
10	IC, 74LS245	965-635-04	4	1A,2A,5C,3A
11	IC, 74LS244	965-635-03	2	4A,4B
12	IC, 74LS04	965-635-00	2	3B,5D
13	IC, 74LS138	965-635-22	2	3C,1K
14	MEMORY EXTENSION ADDRESS PROM	231-7064-00	1	5A
15	IC, OPTION EPROM	231-7071-00	1	4E
16	IC, OPTION EPROM	231-7081-00	1	4F
17	IC, OPTION EPROM	231-7091-00	1	4G
18	IC, 4334P-3HM HITACHI	965-613-13	6	1E,2E,1F,2F,1G, 2G
19	MEMORY EXTENSION PATCH EPROM	231-7063-00	1	4M
20	RES, NTWK, 10K 785-1-R10K	952-010-02	3	RN1,RN2,RN4
21	RES, NTWK, 3.3K (785-1-R3.3K)	950-033-02	1	RN3
22	RES, CARBON 1/4 W ±5%, 1K	942-201-02	13	R1-12,R17
23	RES, CARBON 1/4W ±5%, 150	942-201-51	1	R26
24	RES, CARBON 1/4W ±5%, 330K	942-203-34	2	R27,R24

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, MEMORY EXTENSION "D"	MODEL NO. 235	DATE 1-19-82	231-4462-00 D
		SHEET 4 OF 5	

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, CARBON 1/4W ±5%, 820	942-208-21	6	R18,R23
26	RES, CARBON, 1/4W ±5%, 10K	942-201-03	3	R28,R31,R32
27	RES, CARBON, 1/4W ±5%, 330	942-203-31	2	R29,R30
28	RES, CARBON, 1/4W ±5%, 220K	942-202-24	1	R33
29	RES, CARBON, 1/4W ±5%, 10MEG	942-201-06	1	R25
30	CAP 10pf DM15	915-031-00	1	C54
31	CAP .01 AXIAL.01/50V 180/25V050A	900-021-07	50	C12-52,C55,C56,C65 C59-61,C63,C64,C67
32	CAP 10UF TANT (162D)	916-010-10	5	C9-11,C66,C68
33	CAP 100pf	901-011-01	6	C1-6
34	CAP 15pf DM15	915-031-50	1	C53
35	IC, HI8000	965-613-17	1	1L
36	IC, CLOCK RESTORE FIRMWARE	231-7093-00	1	5H
37	XTAL, 32.768KHZ	967-005-23	1	Y1
38	DIODE, 1N914	961-091-40	4	CR1-4
39	XSTR 2N4250	962-425-00	2	Q10,Q11
40	XSTR MPSA13	964-040-03	1	Q1
41	XSTR 2N3646	962-364-60	6	Q2-7
42	SWITCH, ALCO TPA11FG-PC-2	969-050-16	1	S1
43	CHAS. FSTNR 632B2 (US1590B1)	991-020-26	1	
44	IC, SOCKET, 24 DIP AUGAT (524-AG-37D)	992-010-35	9	5A,4M,5H,4E,4F, 4G,5E,5F,5G
45	SCREW PHMS 6-32 X 1/2 LG	980-632-050	1	
46	WASHER, FLAT #6	986-100-06	1	
47	BATTERY 3.6 N.CAD	975-100-11	1	BT1 INSTALL AT TEST LEVEL
48	WASHER, SPLITLOCK #6	986-200-06	1	

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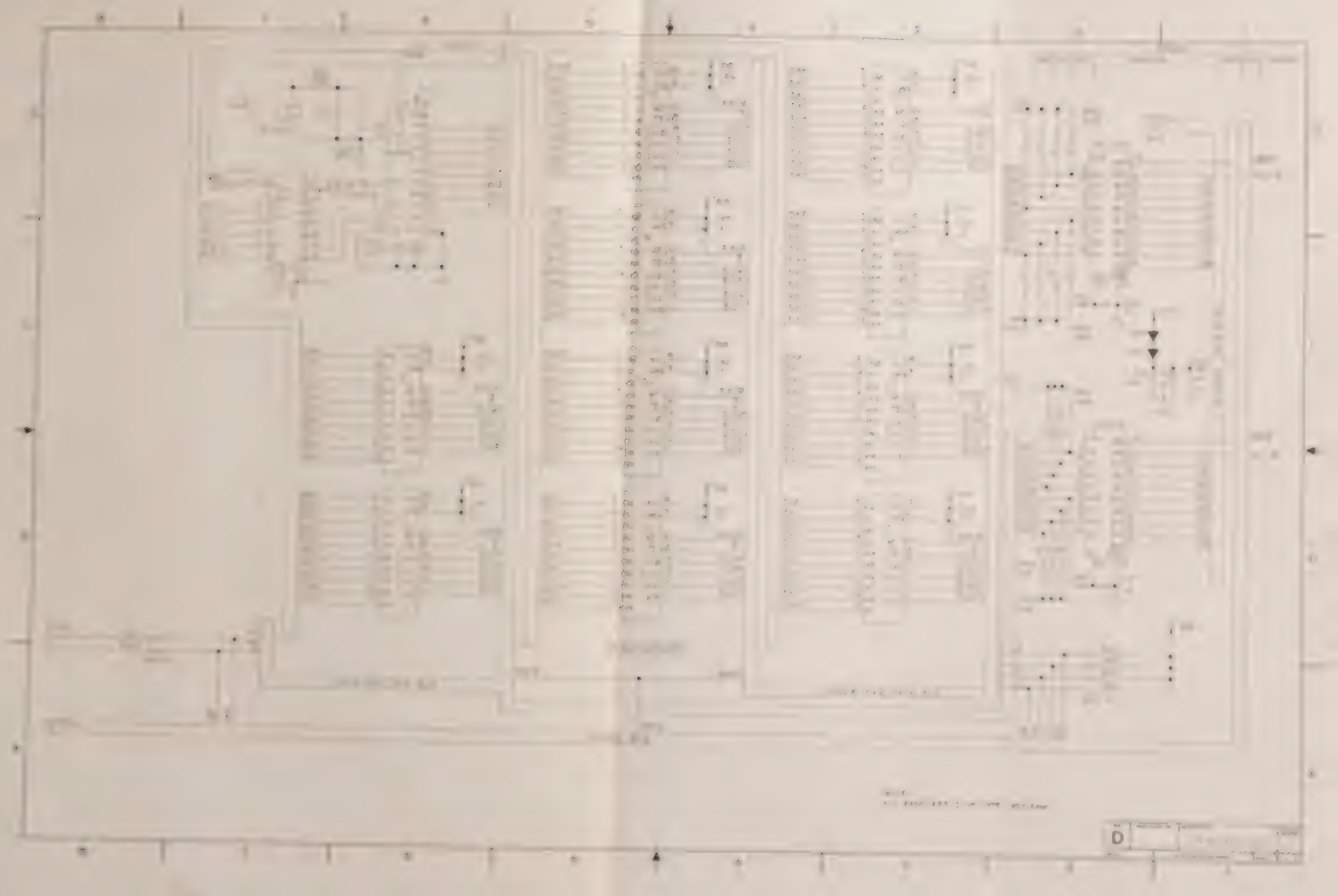
MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
PCB ASSEMBLY, MEMORY EXTENSION "D"		231-4462-00	D
	MODEL NO. 235	DATE 3-18-82	SHEET 5 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	IC, OPTION EPROM	231-7072-00	1	5E
50	IC. OPTION EPROM	231-7082-00	1	5F
51	IC, OPTION EPROM	231-7092-00	1	5G
52				
53				
54				
55				



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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, DIGITAL INPUT BOARD	MODEL NO. 235	231-4350-00	D
		DATE 2-28-80	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB DIGITAL INPUT	231-2350-00	1	
2	SCHEMATIC	231-6350-00	1	
3	TEST SPEC		1	
4				
5				
6	IC, 74LS245 8 BUS XCVR(TI,FC)	965-635-04	1	Z1
7	IC, 74LS42 BCD-DEC DECODER	965-635-20	1	Z2
8	IC, 74LS27 3-3IN POS-NOR(TI,FC	965-635-25	1	Z3
9	IC, 74LS244 8 3-ST DRV(AMD, SIG	965-635-03	1	Z4
10	IC, 74LS10 3-3IN NAND (TI)	965-635-08	1	Z5
11	IC, 74LS04 HEX INV(FC,MO,NL)	965-635-00	1	Z6
12	IC, MC6820 PIA (MOT)(CERAMIC)	965-613-03	3	Z7,8,9
13	IC, 74C30 1-8IN NAND CMOS	965-587-42	7	Z10-13,15-17
14	IC, 74C04(4069)HEX INV CMOS(RC	965-587-05	1	Z14
15	IC, 74C86 4-2IN EXLU OR(CMOS)	965-565-05	15	Z18-32
16				
17				
18				
19				
20				
21				
22				
23	RES, CARBON 1/4W ± 5%, 2.2K	942-202-22	6	R1,5,9,13,17, 21
24	RES, CARBON 1/4W ± 5%, 6.8K	942-206-82	12	R31-36,R2,R6, R10,R14,R18,R22

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

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MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, DIGITAL INPUT BOARD	MODEL NO. 235	231-4350-00	D
		DATE 2-28-80	SHEET 4 OF 5

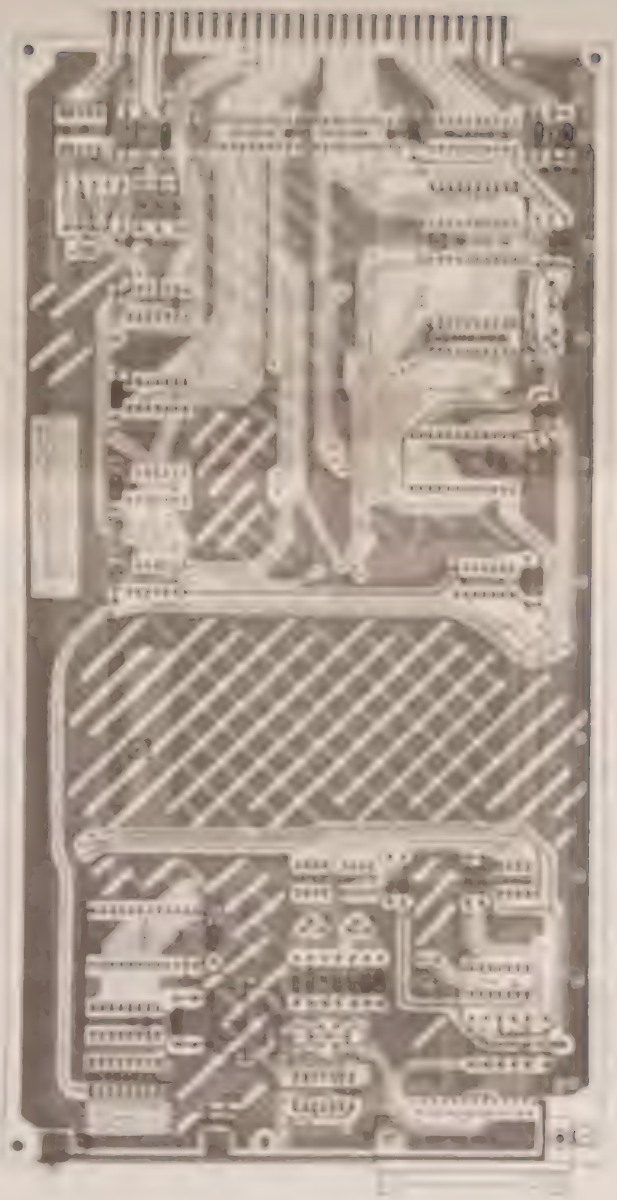
ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, CARBON 1/4W ± 5%, 180	942-201-81	6	R3,R7,R11,R15, R19,R23
26	RES, CARBON 1/4W ± 5%, 2.7K	942-202-72	6	R4,R8,R12,R16 R20,R24
27	RES, CARBON 1/4W ± 5%, 2K	942-202-02	6	R25-30
28	RES, CARBON 1/4W ± 5%, 3.3K	942-203-32	1	R37
29	RES, NTWRK, 15K SIP 785-1-R15K	951-015-02	6	RN1-6
30	RES NTWK, 16PDIP 898-3,R2.2K	951-022-01	6	RN7-12
31				
32				
33				
34				
35	CAP, DISC .01 @ 1KV (5GA-S10)	900-021-05	7	C32 C1,3,5,7,9,11
36	CAP, DISC, .01 @ 500V (5GA)	900-021-04	6	C2,4,6,8,10,12
37	CAP, TANT 22MF @ 10V (162D)	916-022-10	6	C13-18
38	CAP, TANT 10 @ 10V (162D)	916-010-10	2	C20,C31
39	CAP, DISC, 100PF @ 1KV (5GA)	901-011-01	1	C33
40	CAP, AXIAL .01/50V 1801Z5U050A	900-021-07	12	C21-C30, C19, C34
41	CAP NTWRK, .01uF 926CZ5U103M050B	903-100-00	6	CN1-CN6
42				
43				
44	DIODE, ZENER 1N752A (5.6V)	961-075-21	6	CR1-6
45	DIODE, 1N914 (1N4148)(TD,FC,TI	961-091-40	60	CR7-60 CR68-72
46	DIODE, 1N754A (6.8V) (TD,MO)	961-075-41	7	CR61-66,CR73
47				
48				

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY PCB, DIGITAL INPUT BOARD	MODEL NO. 235	231-4350-00	D
		DATE 2-28-80	SHEET 5 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49	SCREW, PHMS 6-32 X 1/2 LG	980-632-050	1	
50	WASHER, FLAT #6	986-100-06	1	
51	WASHER, SPLITLOCK #6	986-200-06	1	
52	XSTR 3646	962-364-60	6	Q1-Q6
53	SWITCH, DIP-6P1T (GH76SB06S)	969-050-13	1	S1
54	SWITCH, DIP-8PIT (GH76SB08S)	969-050-11	1	S2
55	XFMR, ISOLATION	230-7050-00	2	T1,T2
56	OPTO ISO, DUAL(LIT ILCT6-XXX)	000-7540-00	30	Z33-Z62
57	CONN, PC 37 PIN(F) (AMP745108-2)	973-010-78	2	J1,J2
58	CHASSIS FASTENER, 632B2 (US1590B1)	991-020-26	1	
59				
60	SCREW PHMS 4-40 X 3/8 LG	980-440-038	4	J1,J2
61	NUT RADIAL 4-40	984-200-440	4	J1,J2
62	CABLE ASSY, DIGITAL STATUS (J1)	231-5460-00	1	
63	CABLE ASSY, DIGITAL STATUS (J2)	231-5470-00	1	
64	WASHER SPLIT-LOCK #4	986-200-04	4	J1,J2
65	WASHER, FLAT NO. 4	986-100-04	4	J1,J2
66				
67				
68				
69				
70				
71				
72				



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DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

EMERSON

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY, PCB SERIAL I/O RS232C/20MA CURRENT LOOP	MODEL NO. 235	DATE 3-18-80	SHEET 3 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PCB, SERIAL I/O	231-2470-01	1	
2	SCHEMATIC	231-6470-00	1	
3	TEST SPEC		1	
4				
5				
6	IC, MC14411 BIT RATE GEN	965-639-00	1	4G
7				
8	IC, 74LS125	965-635-29	1	2B
9	IC, 74LS27 3-3IN POS-NOR(TI,FC)	965-635-25	1	2C
10	IC, 74LS00 4-2IN NAND (TI)	965-635-07	2	1E,2D
11	IC, 74LS245 8 BUS XCVR(TI,FC)	965-635-04	1	1A
12	IC, 74LS244 8 3-ST DRV(AMD,SIG)	965-635-03	2	2A,3A
13	IC, 74LS04 HEX INV(FC,MO,NL)	965-635-00	1	2E
14	IC, XC6850 ACIA (MOT)	965-613-04	1	1D
15	IC, 6N136	965-570-09	2	2G,3G
16	IC, DS75150J-8	965-642-00	1	1G
17	IC, 1489(RS232C)QUAD LINE RCVR	965-601-00	1	1E
18				
19				
20				
21				
22				
23	RES NETWK, 10K 785-1-R10K	952-010-02	1	RN1
24	RES NETWK, 10K 16DIP(898-3-10K)	951-010-01	1	RN2

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
ASSEMBLY, PCB SERIAL I/O RS232C/20MA CURRENT LOOP		231-4470-00	G
	MODEL NO. 235	DATE 3-18-80	SHEET 4 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
25	RES, CARBON 1/4W ± 5%, 20K	942-202-03	1	R11
26	RES, CARBON 1/4W ± 5%, 15M	942-201-56	1	R4
27	RES, CARBON 1/4W ± 5%, 1K	942-201-02	2	R17,R18
28	RES, CARBON 1/4W ± 5%, 33K	942-203-33	3	R5,R12,R19
29	RES, CARBON 1/4W ± 5%, 4.7K	942-204-72	2	R6,R21
30	RES, CARBON 1/4W ± 5%, 330	942-203-31	2	R7,R1
31	RES, CARBON 1/4W ± 5%, 100	942-201-01	2	R10,R20
32	RES, FILM RN55C 1% 82	924-308-20	1	R9
33	RES, CARBON 1/4W ± 5% 10K	942-201-03	2	R2,R3
34	RES, CARBON 1/4W ± 5% 22K	942-202-23	1	R8
35	RES, CARBON 1/4W ± 5% 2.2K	942-202-22	1	R14
36	RES, CARBON 1/4W ± 5% 130Ω	942-201-31	1	R13
37				
38	CAP, TANT 4.7 @ 35V(196D)	916-470-35	1	C22
39	CAP, DISC, 100 PF @ 1KV (5GA)	901-011-01	2	C6,C27
40	CAP, .01MF	900-021-07	18	C4,5,7,10-14, C16-21,C23-26
41	CAP, TANT 10 @ 10V (162D)	916-010-10	2	C1, C15
42	CAP, DISC, .01 @ 500V (5GA)	900-021-04	1	C28
43	CAP, DISC, 330PF @ 1KV (5GA)	901-013-31	2	C2,C3
44	CAP, TANT 10 @ 25V (162D)	916-110-25	2	C8,C9
45				
46	DIODE, ZENER 1N5226 3.3V	961-522-60	2	CR5,CR7
47	DIODE, 1N4933(1A/50V,FAST)(MO)	961-493-30	4	CR1-4
48				

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3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
ASSEMBLY, PCB SERIAL I/O RS232C/20MA CURRENT LOOP	MODEL NO. 235	231-4470-00	G
		DATE 3-18-80	SHEET 5 OF 5

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
49				
50				
51				
52				
53	XSTR, 2N4250 (PNPA)(FC,NL)	962-425-00	2	Q1,Q2
54	XSTR, PN 2907 (PNP)(NSC)	962-290-70	1	Q3
55	XFMR, SERIAL I/O	230-7070-01	1	T1
56	SWITCH, DPDT, 76SD02S (GRAYHILL)	969-050-15	1	S2
57	RECTIFIER, BRIDGE, WL005M(GI)	966-002-26	2	CR6,CR8
58	XTAL, 1.8432 MHz HC-33	967-005-16	1	Y1
59	SWITCH, DIP-8PIT(GH76SB08S)	969-050-11	1	S1
60	CONN, RECEPT 25PIN (AMP745106-2)	973-010-75	1	J1
61				
62				
63	SCREW PHMS 4-40 X 3/8 LG	980-440-038	2	J1
64	NUT RADIAL 4-40	984-200-440	2	J1
65	CHASSIS FASTENER	991-020-26	1	
66	WASHER SPLIT-LOCK #4	986-200-04	2	J1
67	WASHER FLAT #4	986-100-04	2	J1
68	SCREW, PHMS 6-32 X 1/2	980-632-050	1	
69	WASHER, FLAT NO.6	986-100-06	1	
70	WASHER, SPLITLOCK NO.6	986-200-06	1	

ITEM NO	GAGE / TYPE	COLOR	FROM COMP-PIN	FROM CONN TYPE	TO COMP-PIN	TO CONN TYPE	LGTH	SIGNAL IDENT	REMARKS
NOTE: WIRE COLORS GIVEN AS COLOR CODE NUMBERS									
1	28A	0	P1-1	K	P2-1	K	8'	GND	
2	28A	1	P1-2	K	P2-2	K	8'	RYØ	
3	28A	2	P1-3	K	P2-3	K	8'	RY1	
4	28A	3	P1-4	K	P2-4	K	8'	RY2	
5	28A	4	P1-5	K	P2-5	K	8'	RY3	
6	28A	5	P1-6	K	P2-6	K	8'	RY4	
7	28A	6	P1-7	K	P2-7	K	8'	RY5	
8	28A	7	P1-8	K	P2-8	K	8'	RY6	
9	28A	8	P1-9	K	P2-9	K	8'	RY7	
10	28A	9	P1-10	K	P2-10	K	8'	RY8	
11	28A	90	P1-11	K	P2-11	K	8'	RY9	
12	28A	91	P1-12	K	P2-12	K	8'	RY10	
13	28A	92	P1-13	K	P2-13	K	8'	RY11	
14	28A	93	P1-14	K	P2-14	K	8'	RY12	
15	28A	94	P1-15	K	P2-15	K	8'	RY13	
16	28A	95	P1-16	K	P2-16	K	8'	RY14	
17	28A	96	P1-17	K	P2-17	K	8'	RY15	
18	28A	97	P1-18	K	P2-18	K	8'	GND	
19									
20									
21	28A	901	P1-20	K	P2-20	K	8'	+5VIB	
22	28A	902	P1-21	K	P2-21	K	8'	+5VIB	
23	28A	903	P1-22	K	P2-22	K	8'	+5VIB	
24	28A	904	P1-23	K	P2-23	K	8'	STROBE	
25	28A	905	P1-24	K	P2-24	K	8'	STROBE ENABLE	

ITEM NO	GAGE / TYPE	COLOR	FROM COMP-PIN	FROM CONN TYPE	TO COMP-PIN	TO CONN TYPE	LGTH	SIGNAL IDENT	REMARKS
26	28A	906	P1-25	K	P2-25	K	8'	DI3	
27	28A	907	P1-26	K	P2-26	K	8'	DI2	
28	28A	908	P1-27	K	P2-27	K	8'	DI1	
29	28A	912	P1-28	K	P2-28	K	8'	DIØ	
30	28A	913	P1-29	K	P2-29	K	8'	GND	
31	28A	914	P1-30	K	P2-30	K	8'	GND	
32	28A	915	P1-31	K	P2-31	K	8'	GND	
33	28A	916	P1-32	K	P2-32	K	8'	GND	
34	28A	917	P1-33	K	P2-33	K	8'	GND	
35	28A	918	P1-34	K	P2-34	K	8'	GND	
36	28A	923	P1-35	K	P2-35	K	8'	GND	
37	28A	924	P1-36	K	P2-36	K	8'	GND	
38	28A	925	P1-37	K	P2-37	K	8'	NOT USED	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLE PER DORIC SPEC 000-1003.

2. CUT UNUSED WIRES BACK TO CABLE JACKET.

3. INSTALL A 3/4" LONG PIECE OF SHRINK TUBING, ITEM 8, OVER JACKET AT EACH END OF CABLE.

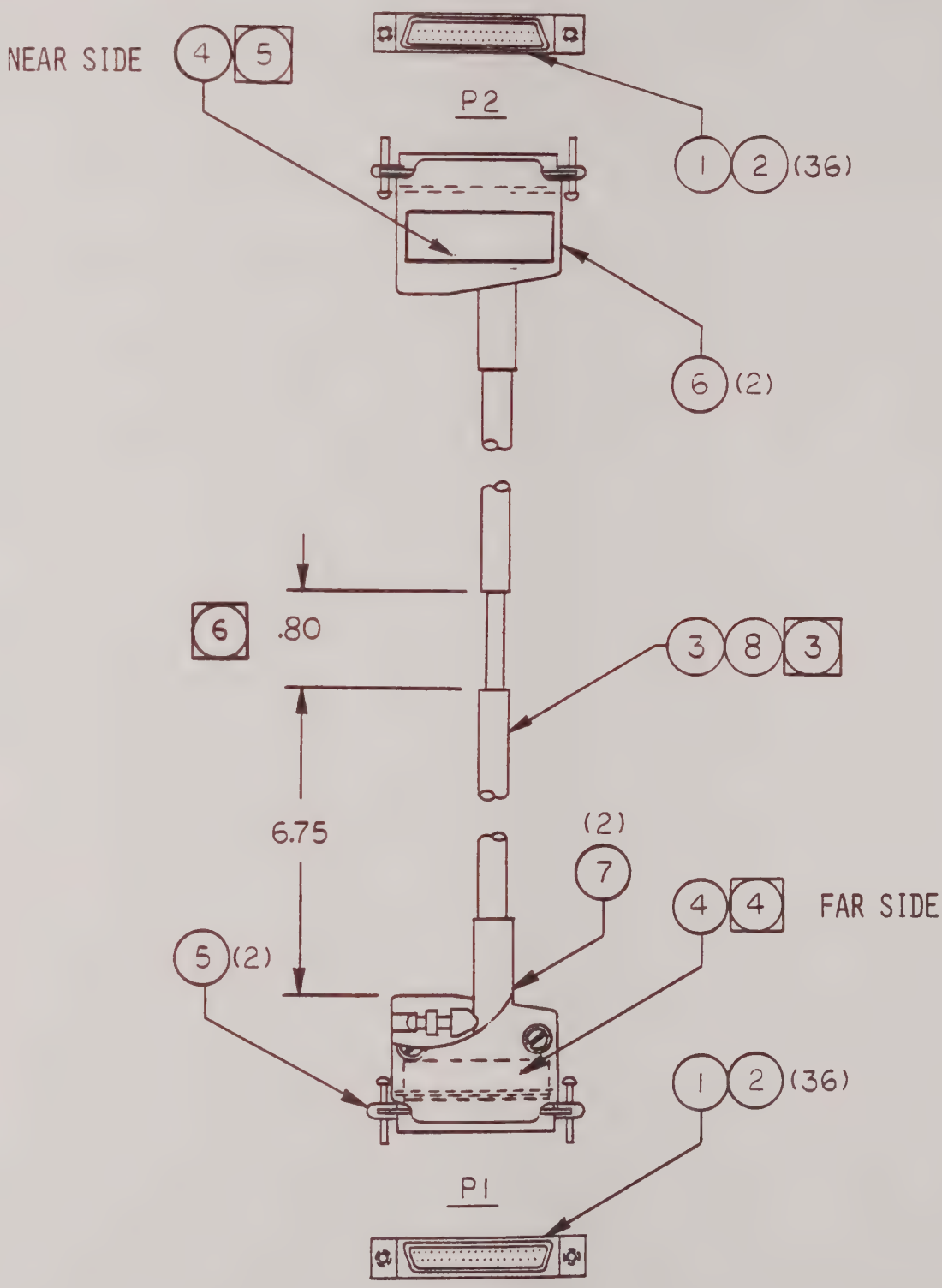
4. TYPE CONNECTOR LABEL WITH "P1/P2 235 ALARM I/O" AND APPLICABLE ASSEMBLY NO. INSTALL ON FAR SIDE.

5. TYPE CONNECTOR LABEL WITH "P2 RLY PNL" AND APPLICABLE ASSEMBLY NO. INSTALL ON THIS SIDE.

6. CUT JACKET TO EXPOSE SHIELD AS INDICATED. DO NOT CUT SHIELD.

TITLE. CABLE ASSY, ALARM I/O TO RELAY PANEL	DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO. 3883 RUFFIN ROAD • SAN DIEGO CA 92123
	DWG NO. 231-5450-00 C
	SHEET 4 OF 6

MDE 11 79 003 DORIC



TITLE:

CABLE ASSY, ALARM I/O TO RELAY PANEL

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO CA 92123

DWG NO. 231-5450-00 C

SHEET 5 OF 6

MDE 11-79 003 DORIC

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
CABLE ASSY, ALARM I/O TO RELAY PANEL	MODEL NO. 235	DATE 7-11-80	SHEET 6 OF 6
		231-5450-00	C

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PLUG ASSY,37MALE (AMP205210-1)	973-010-86	2	
2	PIN CONTACT, CRIMP (AMP66507-9)	973-100-59	72	
3	CABLE 37 (NAT. NQ3728SJ)	900-100-01	8'	
4	LABEL, CONNECTOR ID	000-707-00	2	
5	RETAINER MALE(AMP 205980-1)	973-010-59	2	
6	CABLE CLAMP ASSY(AMP 205731-1)	973-010-95	2	
7	CABLE SLEEVE, #8(AMPH9779513-8)	991-030-03	2	
8	TUBING, SHRINK BLU/BLK 3/8" OD	979-100-375	1 1/2"	

ITEM NO	GAGE TYPE	COLOR	FROM COMP-PIN	FROM CONN TYPE	TO COMP-PIN	TO CONN TYPE	LGTH	SIGNAL IDENT	REMARKS
NOTE: WIRE COLORS GIVEN AS COLOR CODE NUMBERS									
1	28A	0	P1-31	K	----	N	8'	GND -5	
2	28A	1	P1-13	K	----	N	8'	5-1(1)	
3	28A	2	P1-30	K	----	N	8'	5-2(2)	
4	28A	3	P1-12	K	----	N	8'	5-3(4)	
5	28A	4	P1-29	K	----	N	8'	5-4(8)	
6	28A	5	P1-11	K	----	N	8'	5-5(1)	
7	28A	6	P1-28	K	----	N	8'	5-6(2)	
8	28A	7	P1-10	K	----	N	8'	5-7(4)	
9	28A	8	P1-27	K	----	N	8'	5-8(8)	
10	28A	9	P1-8	K	----	N	8'	READY -5	
11	28A	90	P1-26	K	----	N	8'	BUSY -5	
12	28A	91	P1-7	K	----	N	8'	GND -5	
13	28A	92	P1-25	K	----	N	8'	GND -6	
14	28A	93	P1-6	K	----	N	8'	6-1(1)	
15	28A	94	P1-24	K	----	N	8'	6-2(2)	
16	28A	95	P1-5	K	----	N	8'	6-3(4)	
17	28A	96	P1-23	K	----	N	8'	6-4(8)	
18	28A	97	P1-4	K	----	N	8'	6-5(1)	
19	28A	98	P1-22	K	----	N	8'	6-6(2)	
20	28A	901	P1-3	K	----	N	8'	6-7(4)	
21	28A	902	P1-21	K	----	N	8'	6-8(8)	
22	28A	903	P1-2	K	----	N	8'	READY -6	
23	28A	904	P1-20	K	----	N	8'	BUSY -6	
24	28A	905	P1-1	K	----	N	8'	GND -6	

ITEM NO	GAGE / TYPE	COLOR	FROM COMP-PIN	FROM CONN TYPE	TO COMP-PIN	TO CONN TYPE	LGTH	SIGNAL IDENT	REMARKS
25	28A	906	P1-37	K	----	N	8'	GND -4	
26	28A	907	P1-19	K	----	N	8'	4-1(1)	
27	28A	908	P1-36	K	----	N	8'	4-2(2)	
28	28A	912	P1-18	K	----	N	8'	4-3(4)	
29	28A	913	P1-35	K	----	N	8'	4-4(8)	
30	28A	914	P1-17	K	----	N	8'	4-5(1)	
31	28A	915	P1-34	K	----	N	8'	4-6(2)	
32	28A	916	P1-16	K	----	N	8'	4-7(4)	
33	28A	917	P1-33	K	----	N	8'	4-8(8)	
34	28A	918	P1-15	K	----	N	8'	READY -4	
35	28A	923	P1-32	K	----	N	8'	BUSY -4	
36	28A	924	P1-14	K	----	N	8'	GND -4	

NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY PER DORIC SPEC 000-1003.

2. CUT UNUSED WIRES BACK TO JACKET.

3. NO CONNECTION ON THIS END (CUSTOMER CONFIGURED).

4. INSTALL A 3/4" LONG PIECE OF SHRINK TUBING, ITEM 8, OVER JACKET AT EACH END OF CABLE.

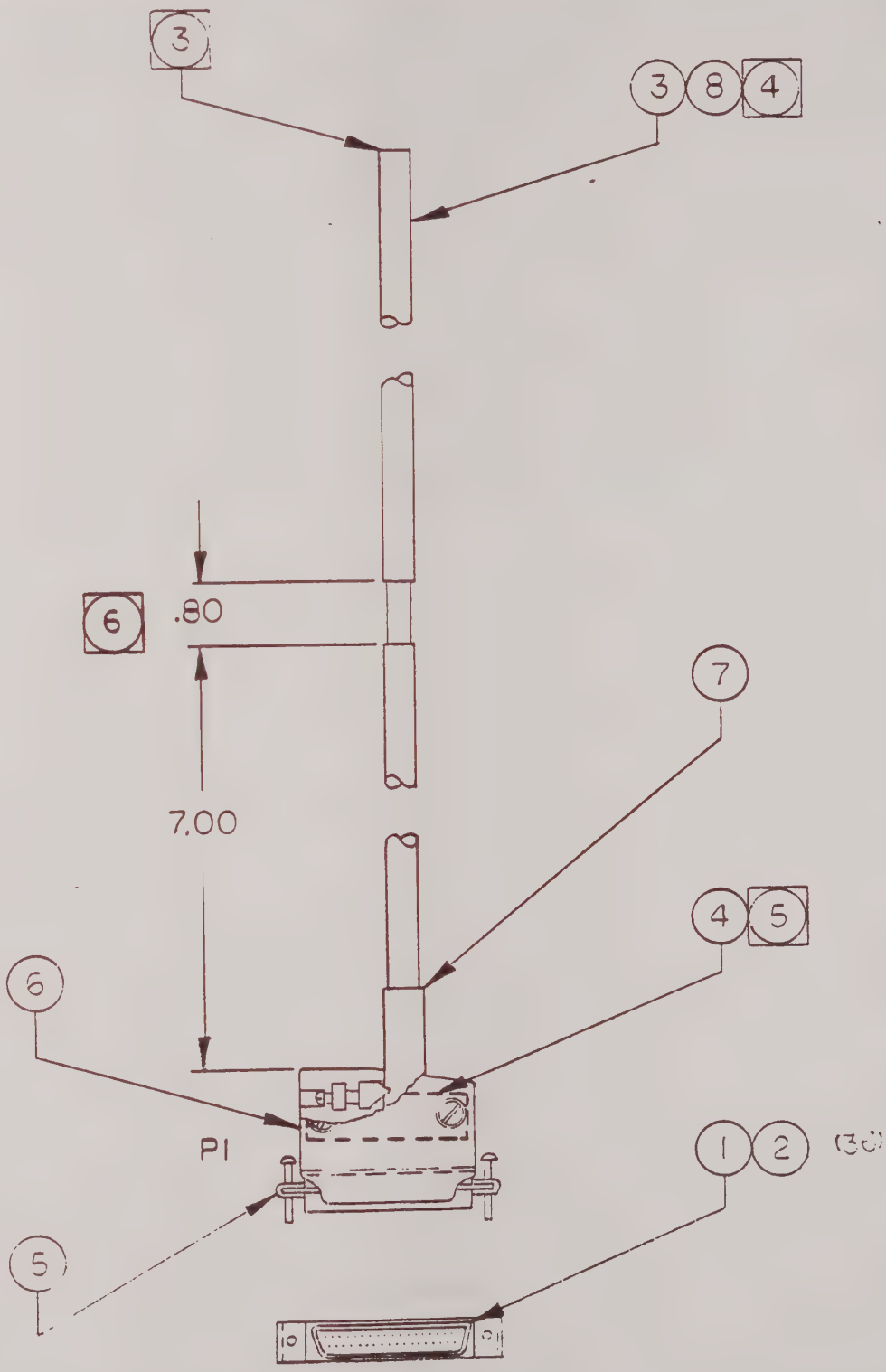
5. TYPE CONNECTOR LABEL WITH "P1 235 DIGITAL STATUS" AND APPLICABLE ASSEMBLY NO. INSTALL ON FAR SIDE.

6. CUT JACKET TO EXPOSE SHIELD AS INDICATED. DO NOT CUT SHIELD.

7. SPECIFIC WORD DESIGNATION AND PIN OUT CAN BE FOUND IN SECTION 3 IN THE OPERATORS MANUAL (DWG 231-4000-XX).

TITLE CABLE ASSY, DIGITAL STATUS (P1)	DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO. 3883 RUFFIN ROAD • SAN DIEGO CA 92123
	DWG NO 231-5460-00 E
	SHEET 4 OF 6

MDE 11 79 003 DORIC



TITLE:

CABLE ASSY, DIGITAL STATUS (P1)

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

DWG NO. 231-5460-00 E

SHEET 5 OF 6

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
CABLE ASSY, DIGITAL STATUS (P1)	MODEL NO. 235	231-5460-00	E
		DATE 7-11-80	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PLUG ASSY, 37 MALE AMP(205-210-1	973-010-86	1	
2	PIN CONTACT CRIMP (AMP66507-9)	973-100-59	36	
3	CABLE 37 (NAT. NQ3728SJ)	900-100-01	8'	
4	LABEL, CONNECTOR ID	000-707-00	1	
5	RETAINER MALE (AMP205980-1)	973-010-59	1	
6	CABLE CLAMP ASSY, AMP (205-731-1	973-010-95	1	
7	CABLE SLEEVE, #8(AMPH9779513-8	991-030-03	1	
8	TUBING, SHRINK BLU/BLK 3/8" OD	979-100-375	1 1/2"	

ITEM NO	GAGE / TYPE	COLOR	FROM COMP-PIN	FROM CONN TYPE	TO COMP-PIN	TO CONN TYPE	LGTH	SIGNAL IDENT	REMARKS
NOTE: WIRE COLORS GIVEN AS COLOR CODE NUMBERS									
1	28A	0	P2-31	K	----	N	8'	GND -2	
2	28A	1	P2-13	K	----	N	8'	2-2(1)	
3	28A	2	P2-30	K	----	N	8'	2-2(2)	
4	28A	3	P1-12	K	----	N	8'	2-3(4)	
5	28A	4	P2-29	K	----	N	8'	2-4(8)	
6	28A	5	P2-11	K	----	N	8'	2-5(1)	
7	28A	6	P2-28	K	----	N	8'	2-6(2)	
8	28A	7	P2-10	K	----	N	8'	2-7(4)	
9	28A	8	P2-27	K	----	N	8'	2-8(8)	
10	28A	9	P2-8	K	----	N	8'	READY -2	
11	28A	90	P2-26	K	----	N	8'	BUSY -2	
12	28A	91	P2-7	K	----	N	8'	GND -2	
13	28A	92	P2-25	K	----	N	8'	GND -3	
14	28A	93	P2-6	K	----	N	8'	3-1(1)	
15	28A	94	P2-24	K	----	N	8'	3-2(2)	
16	28A	95	P2-5	K	----	N	8'	3-3(4)	
17	28A	96	P2-23	K	----	N	8'	3-4(8)	
18	28A	97	P2-4	K	----	N	8'	3-5(1)	
19	28A	98	P2-22	K	----	N	8'	3-6(2)	
20	28A	901	P2-3	K	----	N	8'	3-7(4)	
21	28A	902	P2-21	K	----	N	8'	3-8(8)	
22	28A	903	P2-2	K	----	N	8'	READY -3	
23	28A	904	P2-20	K	----	N	8'	BUSY -3	
24	28A	905	P2-1	K	----	N	8'	GND -3	
25	28A	906	P2-37	K	----	N	8'	GND -1	

ITEM NO	GAGE / TYPE	COLOR	FROM COMP-PIN	FROM CONN TYPE	TO COMP-PIN	TO CONN TYPE	LGTH	SIGNAL IDENT	REMARKS
26	28A	907	P2-19	K	----	N	8'	1-1(1)	
27	28A	908	P2-36	K	----	N	8'	1-2(2)	
28	28A	912	P2-18	K	----	N	8'	1-3(4)	
29	28A	913	P2-35	K	----	N	8'	1-4(8)	
30	28A	914	P2-17	K	----	N	8'	1-5(1)	
31	28A	915	P2-34	K	----	N	8'	1-6(2)	
32	28A	916	P2-16	K	----	N	8'	1-7(4)	
33	28A	917	P2-33	K	----	N	8'	1-8(8)	
34	28A	918	P2-15	K	----	N	8'	READY -1	
35	28A	923	P2-32	K	----	N	8'	BUSY -1	
36	28A	924	P2-14	K	----	N	8'	GND -1	
37									

NOTES: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLE PER DORIC SPEC 000-1003.

2. CUT UNUSED WIRES BACK TO JACKET.

3. NO CONNECTIONS ON THIS END. (CUSTOMER CONFIGURED)

4. INSTALL A 3/4" LONG PIECE OF SHRINK TUBING, ITEM 8, OVER JACKET AT EACH END OF CABLE.

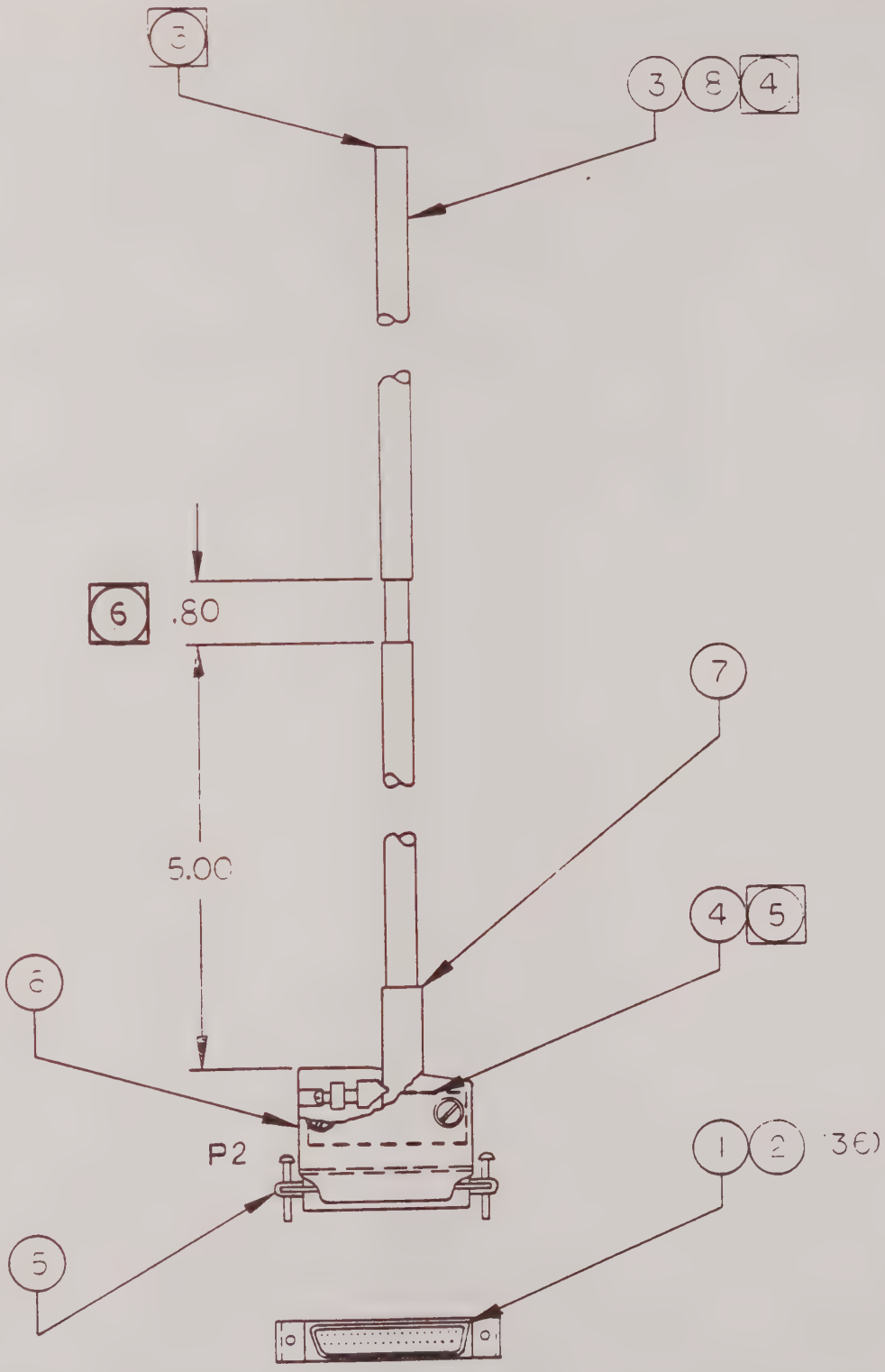
5. TYPE CONNECTOR LABEL WITH "P2 235 DIGITAL STATUS" AND APPLICABLE ASSEMBLY NO. INSTALL ON FAR SIDE.

6. CUT JACKET TO EXPOAE SHIELD AS INDICATED. DO NOT CUT SHIELD.

7. SPECIFIC WORD DESIGNATION AND PIN OUT CAN BE FOUND IN SECTION 3 IN THE OPERATORS MANUAL (DWG 231-4000-XX).

TITLE CABLE ASSY, DIGITAL STATUS (P2)	DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO. 3883 RUFFIN ROAD • SAN DIEGO CA 92123
	DWG NO 231-5470-00 — E
	SHEET 4 OF 6

MDE 11-79 003 DORIC



TITLE:

CABLE ASSY, DIGITAL STATUS (P2)

DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

DWG NO. 231-5470-00 E

SHEET 5 OF 6

MDE 11-79 003 DORIC

DORIC

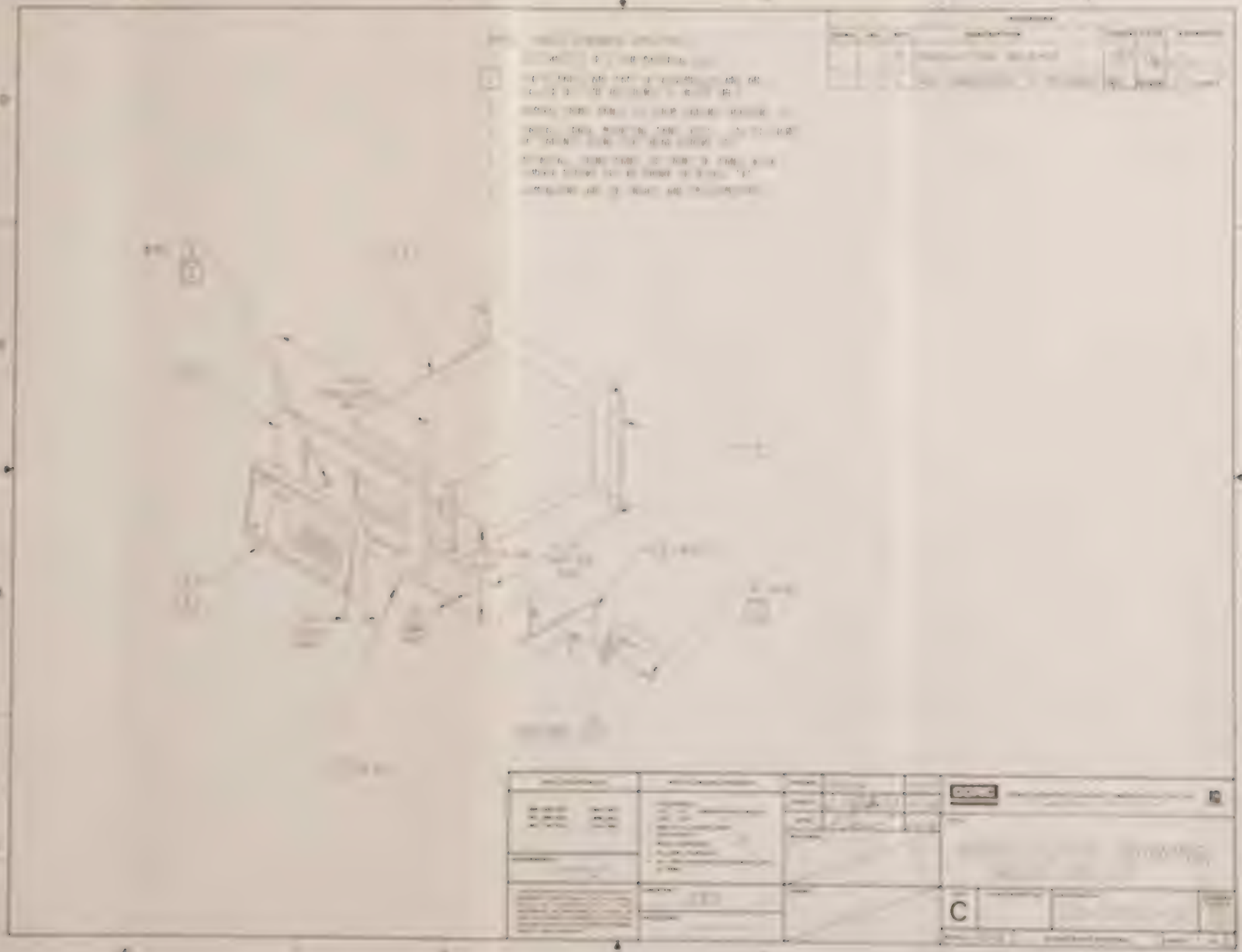
DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

EMERSON

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
CABLE ASSY, DIGITAL STATUS (P2)	MODEL NO. 235	231-5470-00	E
		DATE 7-11-80	SHEET 6 OF 6

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	PLUG ASSY, 37MALE AMP(205-210-1	973-010-86	1	
2	PIN CONTACT CRIMP (AMP66507-9)	973-100-59	36	
3	CABLE 37(NAT. 3728SJ)	900-100-01	8'	
4	LABEL, CONNECTOR ID	000-707-00	1	
5	RETAINER MALE(AMP205980-1)	973-010-59	1	
6	CABLE CLAMP ASSY, AMP(205-731-1	973-010-95	1	
7	CABLE SLEEVE,#8(AMPH9779513-8	991-030-03	1	
8	TUBING, SHRINK BLU/BLK 3/8"OD.	979-100-375	1 1/2"	
9				
10				



DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV.
INSTALLATION DRAWING, RACK MOUNT	MODEL NO. 235	231-8050-00	C
		DATE	SHEET 2 OF 2

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	ASSY, DIGITREND 235	231- 0000-01	1	
2	FRONT PANEL	---	-	2
3	ASSY, PANEL - RACK MOUNT	231-4720-00	1	
4	RACK (CUSTOMER SUPPLIED)	---	—	REF
5	SCREW, FLAT HD PHILLIPS 8-32 X 1/2 LG	---	—	2
6	SCREW, PAN HD PHILLIPS 6-32 X 3/4 LG	---	-	2
7	SCREW, (CUSTOMER SUPPLIED)	----	---	REF
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
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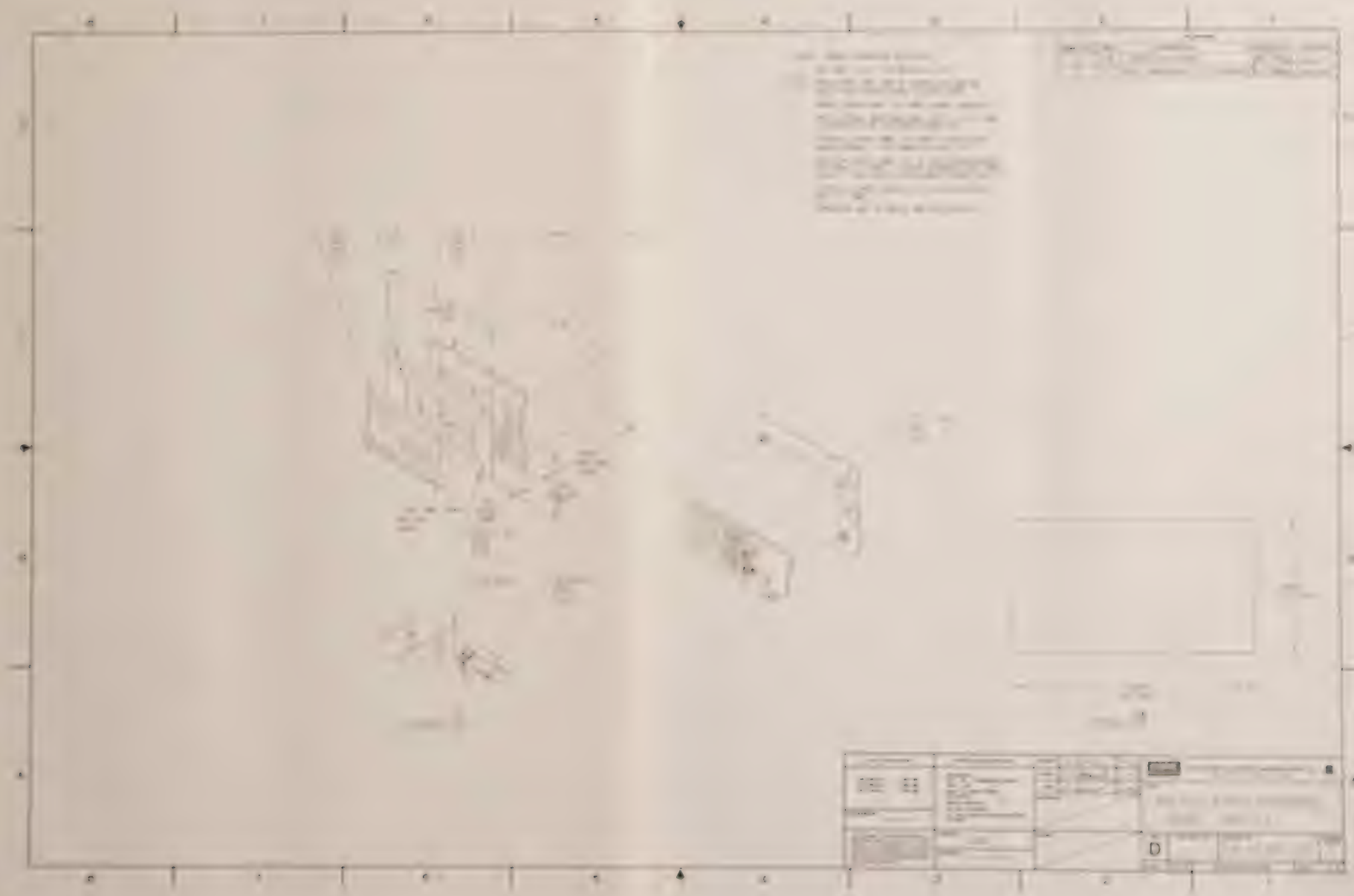
23				
24				

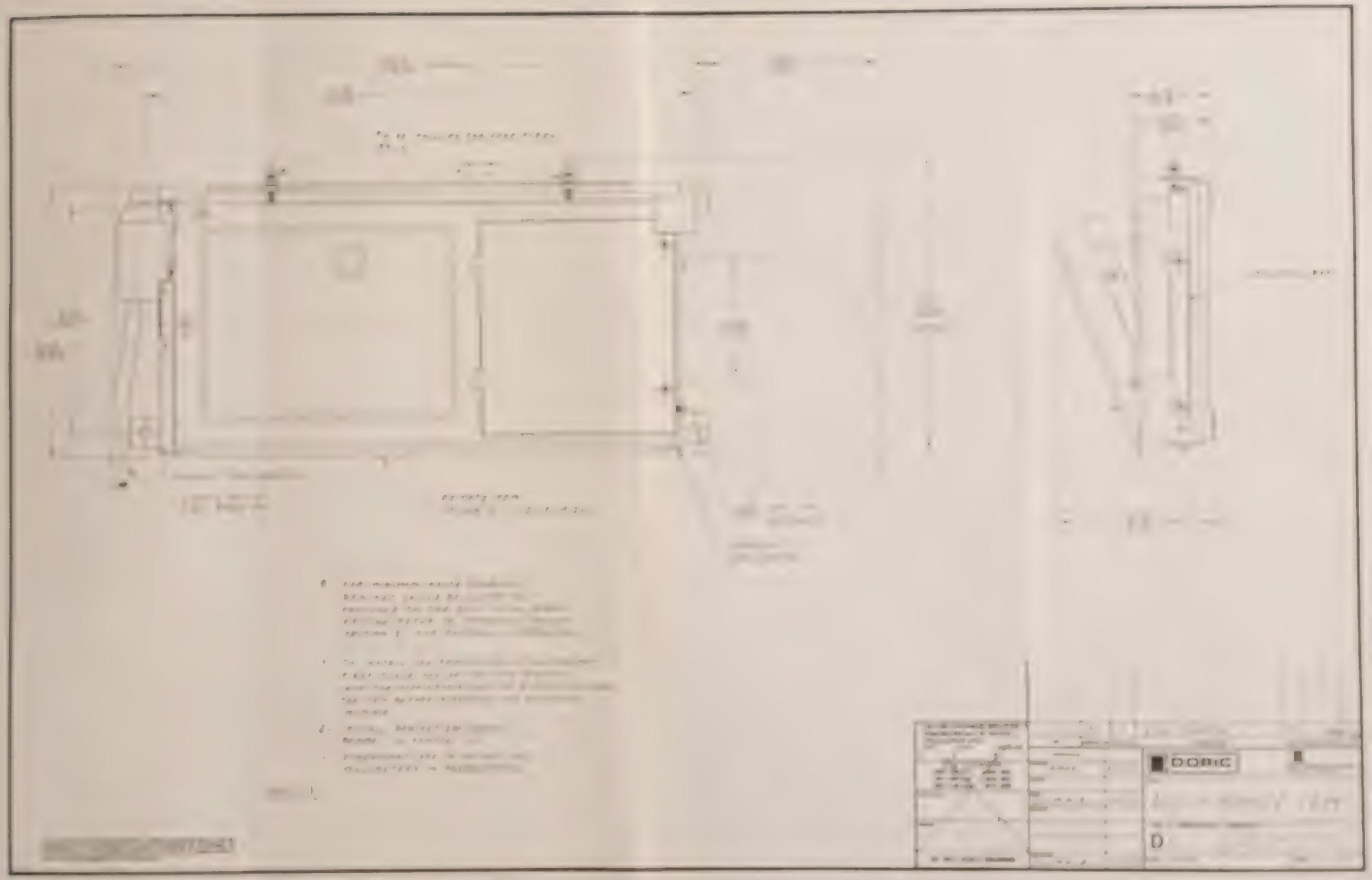


DORIC SCIENTIFIC DIVISION • EMERSON ELECTRIC CO.
3883 RUFFIN ROAD • SAN DIEGO, CA 92123

MATERIAL LIST

DRAWING TITLE	ML	DRAWING NO.	REV
INSTALLATION DRAWING, PANEL MOUNT	MODEL NO. 235	231-8055-00	C
		DATE	SHEET 2 OF 2

ITEM NO.	DRAWING TITLE	DRAWING NO.	NO. REQ.	REMARKS
1	ASSY, DIGITREND-235	231-0000-01	1	
2	FRONT PANEL	---	-	2
3	ASSY, PLATE - PANEL MOUNT	231-4730-00	1	
4	PANEL, (CUSTOMER SUPPLIED)	---	-	REF
5	SCREW, FLAT HD PHILLIPS 8-32 X 1/2 LG	---	-	2
6	SCREW, PAN HD PHILLIPS 6-32 X 3/4 LG	---	-	2
7	CLAMP, PANEL MOUNT	---	-	2
8	SCREW, CLAMP	---	-	2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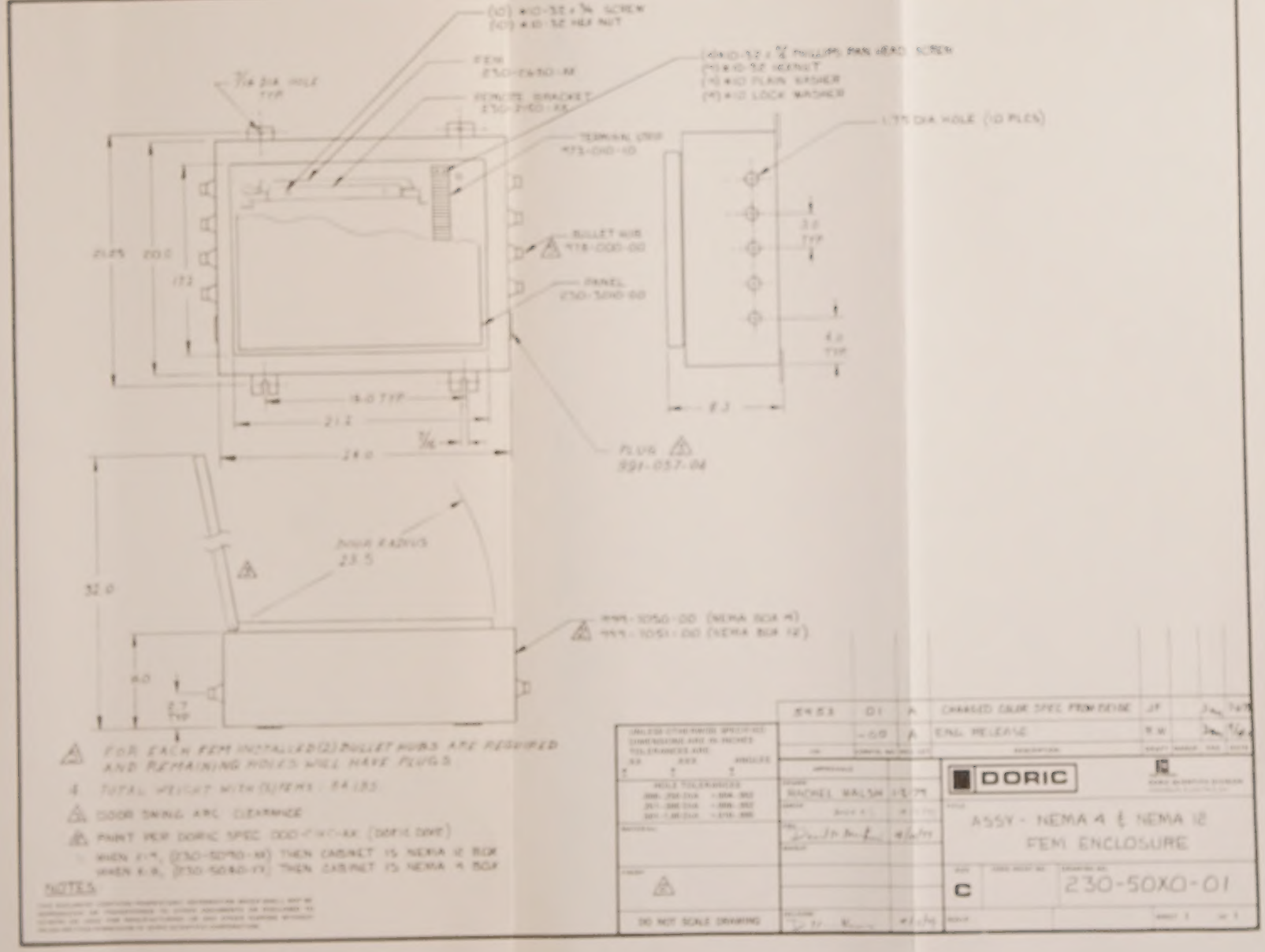
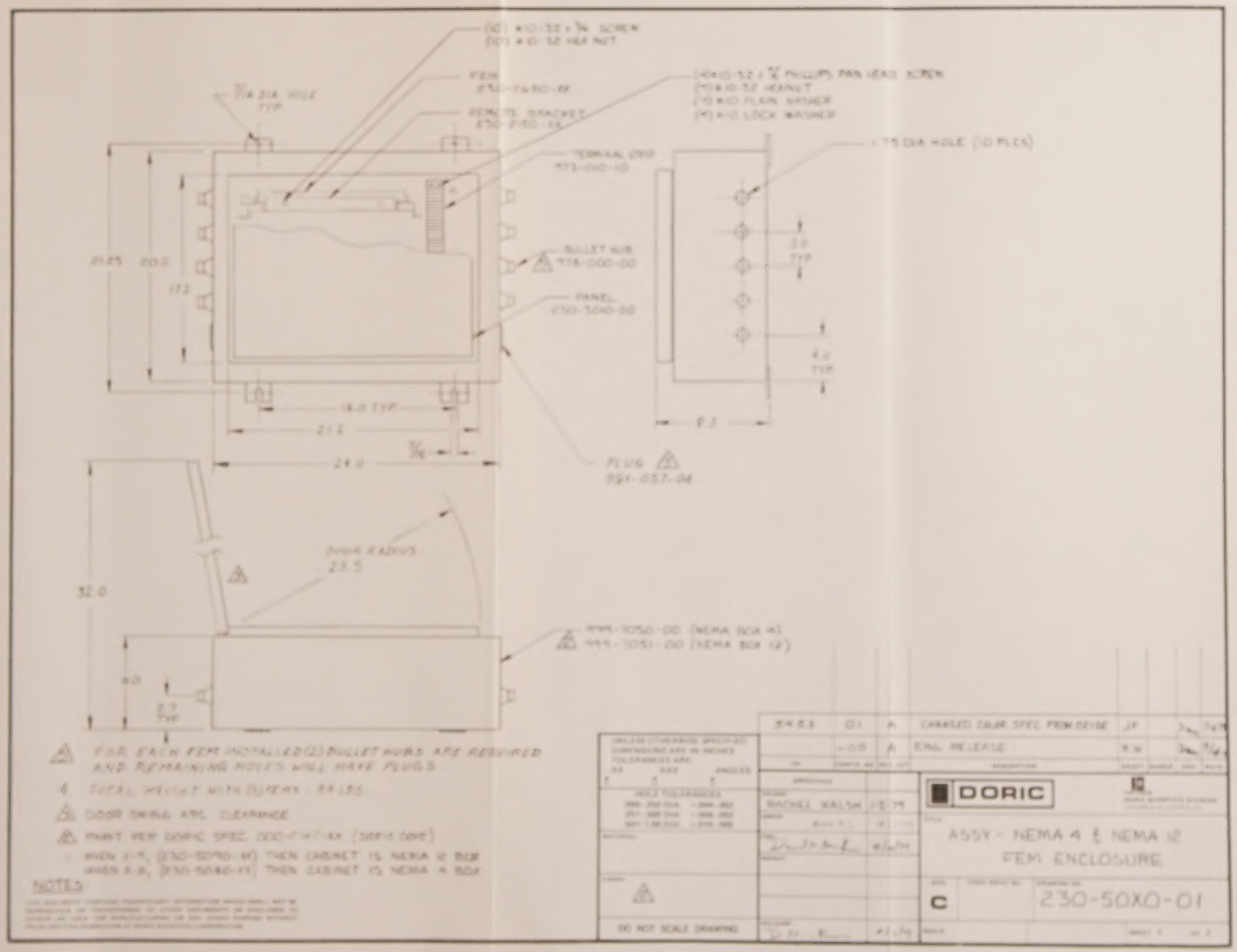


(10) #10-32 x 3/4 SCREW
(10) #10-32 HEX NUT
FEM
230-2650-XX
FEMCTE BRACKET
230-2150-XX
(4) #10-32 x 3/4 PHILLIPS PAN HEAD SCREW
(4) #10-32 HEXNUT
(4) #10 PLAIN WASHER
(4) #10 LOCK WASHER
1.75 DIA HOLE (10 PLCS)
TERMINAL STRIP
973-010-10
BULLET HUB
978-000-00
PANEL
230-3010-00
PLUG
991-037-04
DOOR RADIUS
23.5
999-1050-00 (NEMA BOX 4)
999-1051-00 (NEMA BOX 12)
21.25
20.0
17.2
14.0 TYP
21.2
24.0
32.0
8.3
3.0 TYP
4.0 TYP
FOR EACH FEM INSTALLED (2) BULLET HUBS ARE REQUIRED AND REMAINING HOLES WILL HAVE PLUGS
TOTAL WEIGHT WITH (5) FEMS : 84 LBS
DOOR SWING ARC CLEARANCE
PAINT PER DORIC SPEC 000-CHC-XX (DORIC DIVE)
WHEN X-9, (230-5090-XX) THEN CABINET IS NEMA 12 BOX
WHEN X-8, (230-5080-XX) THEN CABINET IS NEMA 4 BOX
NOTES
DO NOT SCALE DRAWING
5453 01 A CHANGED COLOR SPEC FROM BEIGE
-00 A ENG RELEASE
DORIC
RACHEL WALSH
ASSY - NEMA 4 & NEMA 12
FEM ENCLOSURE
C
230-50X0-01



(10) #10-32 x 3/4 SCREW
(10) #10-32 HEX NUT
FEM
REMOTE BRACKET
TERMINAL STRIP
973-010-10
BULLET HUB
978-000-00
PANEL
230-3010-00
PLUG
991-057-04
1.75 DIA HOLE (10 PLCS)
DOOR RADIUS
23.5
999-3050-00 (NEMA BOX 4)
999-3051-00 (NEMA BOX 12)
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ASSY - NEMA 4 & NEMA 12
FEM ENCLOSURE
C
230-50XO-01

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